DOCKET NO. BASAVANHALLY 38-2-11 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Nagesh R. Basavanhally, *et al.*	Group No.:	2841
Serial No.:	11/444,860	Examiner:	Xiaoliang Chen
Filed:	May 31, 2006	Confirmation No:	7544
For:	PACKAGES WITH BURIED ELECTRICAL LFEEDTHROUGHS		
Appeal No.:	2009-015132		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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March 2, 2011 (Date)

Elizabeth Schumacher
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/Elizabeth Schumacher/
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Sir:

STATUS INQUIRY

Please advise us as to the status of the above-referenced patent application in which an Appeal Brief was filed on March 6, 2009 and a Reply Brief was filed on August 3, 2009.

Respectfully submitted,

HITT GAINES, P.C.

/Ronald J. Corbett/
Ronald J. Corbett
Registration No. 47,500

Date: March 2, 2011
Hitt Gaines, P.C.
P.O. Box 832570
Richardson, Texas 75083-2570
(972) 480-8800

Electronic Acknowledgement Receipt

EFS ID:	9568687
Application Number:	11444860
International Application Number:	
Confirmation Number:	7544
Title of Invention:	Backages with buried electrical feedthroughs
First Named Inventor/Applicant Name:	Nagesh R. Basavanhally
Customer Number:	47394
Filer:	Ronald J. Corbett/Elizabeth Schumacher
Filer Authorized By:	Ronald J. Corbett
Attorney Docket Number:	BASAVANHALLY 38-2-11
Receipt Date:	02-MAR-2011
Filing Date:	31-MAY-2006
Time Stamp:	14:04:54
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for status of Application	basavanhally37_statusinquiry.pdf	72392 a8bb6a91dbfd17648cdf751dc9249c0d4b8b924c	no	1

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Total Files Size (in bytes):	72392

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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Sir:

STATUS INQUIRY

Please advise us as to the status of the above-referenced patent application in which an Appeal Brief was filed on March 6, 2009 and a Reply Brief was filed on August 3, 2009.

Respectfully submitted,

HITT GAINES, P.C.

/Ronald J. Corbett/
Ronald J. Corbett
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Date: September 16, 2010
Hitt Gaines, P.C.
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Electronic Acknowledgement Receipt

EFS ID:	8433815
Application Number:	11444860
International Application Number:	
Confirmation Number:	7544
Title of Invention:	Backages with buried electrical feedthroughs
First Named Inventor/Applicant Name:	Nagesh R. Basavanhally
Customer Number:	47394
Filer:	Ronald J. Corbett/Elizabeth Schumacher
Filer Authorized By:	Ronald J. Corbett
Attorney Docket Number:	BASAVANHALLY 38-2-11
Receipt Date:	16-SEP-2010
Filing Date:	31-MAY-2006
Time Stamp:	15:28:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for status of Application	Status_Inquiry.pdf	88653 9baf2f89e3d4a9b6a6e54921631928f1fa8a4e52	no	1

Warnings:	
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Total Files Size (in bytes):	88653

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Nagesh R. Basavanhally, *et al.*	Group No.:	2841
Serial No.:	11/444,860	Examiner:	Xiaoliang Chen
Filed:	May 31, 2006	Confirmation No:	7544
For:	PACKAGES WITH BURIED ELECTRICAL LFEEDTHROUGHS		
Appeal No.:	2009-015132		

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/Elizabeth Schumacher/
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Sir:

STATUS INQUIRY

Please advise us as to the status of the above-referenced patent application. An Appeal Brief was filed on March 6, 2009 and a Reply Brief was filed on August 3, 2009, and we are awaiting a Decision on this case.

Respectfully submitted,

HITT GAINES, P.C.

/Ronald J. Corbett/
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Electronic Acknowledgement Receipt

EFS ID:	6918898
Application Number:	11444860
International Application Number:	
Confirmation Number:	7544
Title of Invention:	Backages with buried electrical feedthroughs
First Named Inventor/Applicant Name:	Nagesh R. Basavanhally
Customer Number:	47394
Filer:	Ronald J. Corbett/Elizabeth Schumacher
Filer Authorized By:	Ronald J. Corbett
Attorney Docket Number:	BASAVANHALLY 38-2-11
Receipt Date:	01-FEB-2010
Filing Date:	31-MAY-2006
Time Stamp:	12:38:40
Application Type:	Utility under 35 USC 111(a)

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Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for status of Application	Status_Inquiry.pdf	88709 bfc829097881f8ead09612577da04194027 6dd1d	no	1

Warnings:	
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Total Files Size (in bytes):	88709

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/444,860	05/31/2006	Nagesh R. Basavanhally	BASAVANHALLY 38-2-11	7544

47394 7590 09/24/2009

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EXAMINER	
CHEN, XIAOLIANG	

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
09/24/2009	ELECTRONIC

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Appeal No: 2009-015132
Application: 11/444,860
Appellant: Nagesh R. Basavanhally et al.

Board of Patent Appeals and Interferences
Docketing Notice

Application 11/444,860 was received from the Technology Center at the Board on September 14, 2009 and has been assigned Appeal No: 2009-015132.

A review of the file indicates that the following documents have been filed by appellant:

Appeal Brief filed on:	March 06, 2009
Reply Brief filed on:	August 03, 2009
Request for Hearing filed on:	NONE

In all future communications regarding this appeal, please include both the application number and the appeal number.

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By order of the Board of Patent Appeals and Interferences.

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/444,860	05/31/2006	Nagesh R. Basavanhally	BASAVANHALLY 38-2-11	7544

47394 7590 09/10/2009

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EXAMINER	
CHEN, XIAOLIANG	

ART UNIT	PAPER NUMBER
2841	

NOTIFICATION DATE	DELIVERY MODE
09/10/2009	ELECTRONIC

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
11444860	5/31/2006	BASAVANHALLY ET AL.	BASAVANHALLY 38-2-11

HITT GAINES, PC
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RICHARDSON, TX 75083

EXAMINER	
XIAOLIANG CHEN	
ART UNIT	**PAPER**
2841	20090831

DATE MAILED:

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Commissioner for Patents

The reply brief filed on 08-03-09 has been entered and considered. The application has been forwarded to the Board of Patent Appeals and Interferences for decision on the appeal.

/Dean A. Reichard/
Supervisory Patent Examiner, Art Unit 2841

Xiaoliang Chen
Examiner
Art Unit: 2841

DOCKET NO. BASAVANHALLY 38-2-11 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Nagesh R. Basavanhally, *et al.*
Serial No.:	11/444,860
Filed:	May 31, 2006
For:	PACKAGES WITH BURIED ELECTRICAL LFEEDTHROUGHS
Group No.:	2841
Examiner:	Xiaoliang Chen
Confirmation No:	7544

Mail Stop Appeal Brief-Patents

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Sir:

APPELLANTS' REPLY BRIEF UNDER 37 C.F.R. §41.41

In response to the Examiner's Answer mailed June 3, 2009, the Appellants submit this Reply Brief under 37 C.F.R. §41.41.

I. Reply to Examiner's Arguments

1) In response to the Appellants' argument that Dove in view of Yasumura is not a proper combination because Dove teaches away from the Yasumura's channel, the Examiner argues:

> The statement of Dove (C.2, L.13-22) cited by applicant, of which, Dove is used in the background of the invention, and which is unrelated to the modification at all. The Figures used in the argument are not used in the rejection and are not related to the rejection. (Examiner's Answer, Page 17, section (A).

In response, the Appellants respectfully maintain that it is irrelevant whether or not the teachings by Dove are part of Dove's Background section or were used in the Examiner's rejection. The whole of Dove's disclosure reflects the understanding of one of ordinary skill in the art and therefore the whole of Dove's disclosure must be considered. The Examiner can't selectively pick and choose between the various teachings of Dove, ignoring those inconvenient to his arguments. As already explained in the Appeal Brief, Dove teaches the importance of avoiding electrical interference through the use of an integrally shield circuit, and, that inadvertent gaps or spaces can provide openings through which electromagnetic signals undesirably can radiate. In view of these teachings by Dove, one of ordinary skill would not have been motivated to introduce a plurality of Yasumura's channels into Dove's apparatus, as proposed in the Office Action, because this would introduce multiple routes through which undesirable electromagnetic signals could radiate into or out of Dove's apparatus.

2) In response to the Appellants' argument that Dove in view of Yasumura is not a proper combination because there is no reasonable expectation of success of introducing Yasumura's electrical interconnections into Dove's apparatus, the Examiner argues:

> Dove disclose the conductive lead, (Dove's lead is on the surface of the board), Yasumura teaches a feedthrough structure, a channel with a conductive lead, (cut out

> a channel in the board and place the conductive lead in the channel), therefore using Yasumara's feedthrough stucture in Dove's device is performable and reasonable. (Examiner's Answer, Page 17, section (B).

In response, the Appellants respectfully maintain that Yasumara teaches the use of contact wipes which requires the movement of one conductive element against another conductive element to form the contact wipe (see e.g., Illustration 4 in the Appeal Brief), and, there is no evidence provided by the Office Action or Answer that Dove's device could accommodate such wiping motions.

For instance, there is still no explanation of how Yasumura's curved paralleled conductive elements could be reasonably moved to form a contact wipe, in the Examiner's proposed modification to form a channel or gap in Dove's apparatus. For instance, merely cutting out a channel in the board and placing a conductive lead in the channel, as speculated by the Examiner, does not inherently achieve the contact wipe required by Yasumara. For instance, there is no evidence presented to show that Dove's components are designed to accommodate Yasumara's required wiping motions. Rather, Dove's heat sink 115 is attached to the integrated circuit 110 through a hole 140 in the substrate 135 and also directly attached to a side 136 of the substrate 135 (Dove, FIG. 1, illustration 3 herein; C.3, L. , 37-50). Moreover, the conductive layers 145 and dielectric layers 150 are depicted as attached to the substrate 135 and the conductive layers 145 are bonded via wires 155 to the electronic component 110. Given these inter-attached and bonded structures, it is not apparent how pairs of Yasumura's conductive elements could be arranged in channels and so that wiping motions to achieve Yasumura's electrical connections. The Office Action or Answer has not explained how it would be obvious to achieve electrical connections using wiping motions for this combination of references.

3) In response to the Appellants' argument that Dove in view of Yasumura is not a proper combination because there is no articulated reasoning with rational underpinnings to support the combination of Dove in view of Yasumura, the Examiner argues:

> As in the final rejection, examiner clearly stated the motivation to combine the reference of Dove and Yasumara: in order to reduce the size and increase the stability and integrity of structure of the device, and a person having ordinary skill in the art would recognize the motivation easily, since the modification integrating the conductors into the channels of the substrate instead of the conductors laying on the structure of the substrate is well known in the electronic housing art. (Examiner's Answer, Page 17, section (C).

The Appellants agree that the Examiner clearly stated the rejection. However, neither the Office Action nor Answer articulate reasoning with rational underpinnings to support a motivation for the asserted combination. Again, as pointed out in the Appeal Brief, no portions of Dove or Yasumara have been cited to support the assertion that Yasumura's modifications would actually reduce the size or increase structural integrity of Dove's device, as compared to the devices already disclosed in Dove. For instance, it seems that Dove's device would have to be modified, somehow, to accommodate the wiping motions required by Yasumara to achieve a contact wipe. It does not seem that such a modification would this actually reduce the size of Dove's device. For instance, it seems that Dove's device would have to be modified, by cutting out channels in the board as speculated by the Examiner, to accommodate Yasumura's curved paralleled conductive elements. It does not seem that such a modification would this actually increase structural integrity of Dove's device. For these reasons, the Office Action or Answer has not articulated reasoning with rational underpinnings to support this asserted combination of references.

4) In response to the Appellants' argument that Dove does not teach or suggest a hermetically sealed cavity, such as in the apparatus recited in Claim 4, the Examiner's argues:

> a) Again, as pointed out above, applicant using the background of the invention of Dove, which is not related and was not used in the rejection at all.
> b) Dove clearly disclose wherein the joint housing, and substrate hermetically seal the cavity (the metal cover is sealed to the cavity [col. 1, line 43], and shows in figure 1. (Examiner's Answer, Page 18)

In response to point (a), the Appellants again respectfully maintain that it is irrelevant whether or not the teachings by Dove are part of Dove's Background section or were used in the Examiner's rejection. The whole of Dove's disclosure must be considered. The Examiner cannot selectively pick and choose between the various teachings of Dove ignoring those inconvenient to his arguments.

In response to point (b), the Appellants respectfully disagree that Dove clearly discloses a hermetic seal. For instance, the sentence relied upon by the Examiner (C.1, L.43) states:

> One problem attendant with the more traditional method of constructing microwave circuits is that the method of sealing the metal cover to the cavity uses conductive epoxy. (Dove, Col. 1, Lines 40-43)

The Appellants submit that this sentence from Dove does not teach or suggest a hermetically sealed cavity as recited in the pending claim. In partiuclar, disclosing that a metal cover is sealed to a cavity with epoxy does not teach or suggest that the cavity is hermetically sealed, or at least, the Examiner has not shown why such a seal inherently hermetic. If the Examiner is stating that such a seal is hermetic, Applicants request that the Examiner provide evidence for such a conclusion. Additionally, the Appellants submit that there is nothing in Figure 1 of Dove (shown in Illustration 3 of the Appeal Brief) that teaches or suggests a hermetic seal, or at least the Examiner has not shown how this is inherently taught by the figure.

The Appellants also wish to note for the record that the above relied-upon portion of Dove (C.1, L.43) is from the background section of Dove, the very same background section which the Examiner in point (a) and section (1) above asserted, "is not related and was not used in the rejection

at all." It seems, therefore, that the Examiner wishes to use Dove's background when it supports the Examiner's rejection, but ignore Dove's background when it teaches away from the asserted combination of art being made by the Examiner.

5) In response to the Appellants' argument that there is no motive the combine the teaching of Tatum with Dove, Yasumura, Jacob, and Steddom, to suggest the apparatus recited in Claim 5, the Examiner argues:

> a) The teaching of Tatum does not related to any modification of the device of Dove by Yasumura, Jacob, and Steddom.
> b) The motivation is clearly stated in the final rejection that it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the optical device and a window as taught by Tatum et al. in the housing of the electrical device of Dove et al., in order to be able to couple the device to the faster optical communications applications (Tatum et al. paragraph [0002]).

In response, the Applicants maintain that neither the Office Action nor Answer provide reasoning with rational underpinning to explain why one of ordinary skill in the art would replace, or add to Dove's integrated circuit, an array of Tatum's vertical cavity surface emitting lasers. As explained in the Appeal Brief, Dove's device is directed to microwave circuits (e.g., integrated thick film RF and microwave microcircuits). The Office Action provides no reason why one would either replace Dove's microwave integrated circuit located inside of the conductive lid with an array of Tatum's vertical cavity surface emitting lasers or add an array of lasers to Dove's microwave circuit. For instance, neither the Office Action nor Answer provide evidence and reasoning to show that such a replacement actually results in, or has a likelihood of, producing faster optical communications applications in Dove's modified device.

II. Conclusion

For the at least the reasons set forth above and in the appeal brief filed March 6, 2009, the claims on appeal are patentably non-obvious over the references as applied in the final rejection and Examiner's Answer. Accordingly, the Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellant's pending claims.

Respectfully submitted,

HITT GAINES, P.C.

Ronald J. Corbett
Registration No. 47,500

Dated: August 3, 2009

Electronic Acknowledgement Receipt

EFS ID:	5819021
Application Number:	11444860
International Application Number:	
Confirmation Number:	7544
Title of Invention:	Backages with buried electrical feedthroughs
First Named Inventor/Applicant Name:	Nagesh R. Basavanhally
Customer Number:	47394
Filer:	Ronald J. Corbett/Elizabeth Schumacher
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Attorney Docket Number:	BASAVANHALLY 38-2-11
Receipt Date:	03-AUG-2009
Filing Date:	31-MAY-2006
Time Stamp:	17:42:18
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Reply Brief Filed	basavanhally_38_Reply_Brief.pdf	354162 411af72b5380464377b6f8fcca739388023d3870	no	7

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Total Files Size (in bytes):	354162

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/444,860	05/31/2006	Nagesh R. Basavanhally	BASAVANHALLY 38-2-11	7544

47394 7590 06/03/2009

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EXAMINER	
CHEN, XIAOLIANG	

ART UNIT	PAPER NUMBER
2841	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 11/444,860
Filing Date: May 31, 2006
Appellant(s): BASAVANHALLY ET AL.

Elizabeth Schumacher
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03-06-09 appealing from the Office action mailed 08-28-08.

1) Real Party in Interest

A statement identifying by name the real party in interest in contained in the brief.

2) Related Appeals and Interferences

The following are related appeals, interferences, and judicial proceedings known to the examiner which may related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal is contained in the brief.

3) Status of Claims

The statement of the status of claims contained in the brief is correct.

4) Status of Amendments

The appellant's statement of the status of Amendments contained in the brief is correct.

5) Summary of Claimed Subject Matter

The Summary of Claimed Subject Matter contained in the brief is correct.

6) Grounds of Rejection to be reviewed on appeal

The appellant's statement of the Grounds of Rejection to be reviewed on appeal is correct.

7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

8) Evidence Relied Upon

US 6809931	Dove et al.	Oct. 24, 2004
US 7192320	Yasumura et al.	Mar. 20, 2007
US 4811082	Jacobs et al.	Mar. 07, 1989

US 20040080917	Steddom et al.	Apr. 29, 2004
US 20040076205	Tatum et al.	Apr. 22, 2004

9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6-8, 12, 15, 16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove et al. (US6809931) in view of Yasumura et al. (7192320).

Re claim 6, Dove et al. show and disclose

An apparatus, comprising:

a semiconductor substrate (135, fig. 1) having a top surface;

a housing having (160, fig. 1) an inner surface, the top and inner surfaces being located to form a cavity (fig. 1) between the housing and the substrate;

a joint (top of 145, joints 160, fig. 1) between the top surface of the substrate and the housing;

a micro-electronic structure (110, fig. 1) being exposed to the cavity and being located between the substrate and housing (fig. 1);

electrical feedthroughs (middle 145, fig. 1) traversing the joint and being connected to the micro-electronic structure (fig. 1);

a dielectric layer (bottom 150, fig. 1) located over the substrate, portions of the electrical feedthroughs that traverse the joint (fig.1), the dielectric layer insulating the electrical feedthroughs from the substrate (fig. 1); and

a capping dielectric layer (top 150, fig. 1) located on both the electrical feedthroughs and the dielectric layer, and located in-between the dielectric layer and the housing (fig. 1).

Dove et al. does not disclose

the feedthroughs being located in trenches in the dielectric layer.

Yasumura et al. teaches a device wherein

the feedthroughs being located in trenches (FIG. 46 illustrates an electrical device, wherein the paralleled conductive elements or the signal traces are placed respectively into channels in the dielectric layer [col. 15, line 36]) in the dielectric layer.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to place the feedthroughs in the trenches in the dielectric layer as taught by Yasumura et al. in the device of Dove et al., in order to reduce the size and increase the stability and integrity of structure of the device.

Re claim 7, Dove et al. show and disclose

The apparatus of claim 6, wherein the joint, housing, and substrate hermetically seal (the metal cover is sealed to the cavity [1, line 43]) to the cavity.

Re claim 12, Dove et al. show and disclose

A method of packaging a micro-electronic structure, comprising:

forming electrical feedthroughs (middle 145, fig. 1) that connect to a micro-electronic structure (110, fig. 1) located over a substrate (135, fig. 1); and

forming a package (fig. 1) by joining a housing (160, fig. 1) to the substrate such that the micro-electronic structure is exposed to a cavity formed between the housing and the substrate (fig. 1); and

a dielectric layer (150, bottom, fig. 1) being located over the substrate, and forming a capping dielectric layer (150 top, fig. 1) on the electrical feedthrough and the dielectric laver, the capping dielectric laver located in-between the dielectric laver and the housing (fig. 1); and

wherein the joining includes forming a joint (top of 145, joints 160, fig. 1) between the housing and the substrate,

Dove et al. does not disclose

wherein the forming of each electrical feedthrough includes forming a trench in a dielectric layer, depositing conductive material in the trench, and a portion of each trench traversing the joint.

Yasumura et al. teaches a device including

forming of each electrical feedthrough includes forming a trench in a dielectric layer, depositing conductive material in the trench (FIG. 46 illustrates

an electrical device, wherein the paralleled conductive elements or the signal traces are placed respectively into channels in the dielectric layer [col. 15, line 36]), and a portion of each trench traversing the joint.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the feedthroughs in the trenches in the dielectric layer as taught by Yasumura et al. in the device of Dove et al., in order to reduce the size and increase the stability and integrity of structure of the device.

Re claims 8 and 20, Dove et al. show and disclose

The claims 6 and 12 respectively above,

Dove et al. does not disclose

wherein the joint includes a solder joint located between the housing and the dielectric layer.

However, Dove et al. disclose

1) the device is sealed (see claim 7), and the lid 160 and the joint , top of 145, are both made of metal, and 2) Dove et al. disclose a method to seal the device is by soldering (with solder [col. 1, line 37]).

Therefore, it would have been obvious to one having ordinary skill in the art would seal the joint of the device of Dove et al., or at least the joint could be soldered, in order to same time and reduce the cost (Dove et al., col. 1, line 48]).

Re claim 15, Dove et al. show and disclose

The method of claim 12, wherein the forming of each electrical feedthrough includes forming a metallic path (145, fig. 1) over the dielectric layer that electrically connects to the conducting material in one of the trenches; and electrically connecting the paths to the electronic structure (fig. 1).

Re claim 16, Dove et al. show and disclose

The method of claim 12, wherein the joining includes hermetically sealing the cavity (the metal cover is sealed to the cavity [1, line 43]).

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove et al. in view of Yasumura et al. and Jacobs et al. (US4811082).

Re claim 1, Dove et al. show and disclose

An apparatus, comprising:

a substrate (135, fig. 1) having a top surface;

a housing (160, fig. 1) having an inner surface, the top and inner surfaces being located to form a cavity (fig. 1) between the housing and the substrate;

a joint (top of 145, joints 160, fig. 1) between the top surface and the housing;

a micro-electronic structure (110, fig. 1) being exposed to the cavity and being located between the substrate and housing; metal electrical feedthroughs (145s, fig. 1) traversing the joint and being connected to the micro- electronic structure;

a dielectric layer located (150, bottom, fig. 1) over the substrate, and

a capping dielectric layer (150, top, fig. 1) located on both the electrical feedthroughs and the dielectric layer, and located in-between the dielectric layer and the housing (fig. 1),

Dove et al. does not disclose

1) portions of the electrical feedthroughs being located in trenches in the dielectric layer;

2) wherein the metal electrical feedthroughs have a density along part of the joint of at least 10 per millimeter.

Yasumura et al. teaches a device wherein

1) the feedthroughs being located in trenches (FIG. 46 illustrates an electrical device, wherein the paralleled conductive elements or the signal traces are placed respectively into channels in the dielectric layer [col. 15, line 36]) in the dielectric layer.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to place the feedthroughs in the trenches in the dielectric layer as taught by Yasumura et al. in the device of Dove et al., in order to reduce the size and increase the stability and integrity of structure of the device.

Jacobs et al. teaches a device wherein

2) the metal electrical feedthroughs have a density along part of the joint of at least 10 per millimeter. (having very high wiring density (i.e. 5 micron lines on a 10 micron pitch) [col. 9, line 10])

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replacing the electrical feedthroughs of Dove et al. et al. with higher density feedthroughs as taught by Jacobs et al., "to provide an integrated circuit packaging structure which can provide the high circuit density, high speed characteristics of wafer scale integration while high manufacturing yields are possible." (Jacobs et al., [col. 4, line 23])

Re claim 3, Dove et al. show and disclose

The apparatus of claim 1,

Dove et al. does not disclose

the metal electrical feedthroughs have a density along part of the joint of at least 50 per millimeter.

Jacobs et al. teaches a device wherein

the metal electrical feedthroughs have a density along part of the joint of at least 50 per millimeter. (having very high wiring density (i.e. 5 micron lines on a 10 micron pitch) [col. 9, line 10])

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replacing the electrical feedthroughs of Dove et al. et al. with higher density feedthroughs as taught by Jacobs et al., "to provide an integrated circuit packaging structure which can provide the high circuit density, high speed characteristics of wafer scale integration while high manufacturing yields are possible." (Jacobs et al., [col. 4, line 23])

4. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove et al. in view of Yasumura et al. and Jacobs et al. as applied to claim 1 above, and further in view of Steddom et al. (US20040080917).

Re claim 2, Dove et al., Yasumura et al. and Jacobs et al. disclose

The apparatus of claim 1,

Dove et al., Yasumura et al. and Jacobs et al. do not disclose

wherein the metallic electrical feedthroughs have heights normal to the top surface of at least 0.5 micro-meters.

Steddom et al. teaches a device wherein

the metallic electrical feedthroughs have heights (integrating transmission lines (feedthroughs) have a thickness about 5 to about 50 microns [0041]) normal to the top surface of at least 0.5 micro-meters.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replacing the electrical feedthroughs of Dove et al. et al. with same thickness as taught by Jacobs et al., in order to meet the requirements for good impedance control and low insertion loss at high frequencies that reach 100 GHz and higher (Dive et al. paragraph [0041]).

Re claim 4, Dove et al. show and disclose

The apparatus of claim 2, wherein the joint, housing, and substrate hermetically seal the cavity (the metal cover is sealed to the cavity [1, line 43]).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dove et al., Yasumura et al., Jacobs et al. and Steddom et al. as applied to claim 4 above, and further in view of Tatum et al. (US20040076205).

Re claim 5, Dove et al., Yasumura et al., Jacobs et al. and Steddom et al. disclose the apparatus of claim 4,

Dove et al., Yasumura et al., Jacobs et al. and Steddom et al. do not disclose

wherein the micro-electronic structure includes a two-dimension array of optical devices and the housing has a window for passing visible or infrared light through the housing.

Tatum et al. teaches a device wherein

the micro-electronic structure includes a two-dimension array (a two-dimension array [0069]) of optical devices (a vertical cavity surface emitting laser (VCSEL), [0001]) and the housing has a window (a housing window [0028]) for passing visible or infrared light through the housing.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the optical device and a window as taught by Tatum et al. in the housing of the electrical device of Dove et al. et al., in order to be able to couple the device to the faster optical communications applications (Tatum et al. paragraph [0002]).

6. Claims 9, 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove et al. in view of Yasumura et al. as applied to claims 6-8, 12, 15, 16, and 20 above, and further in view of Jacobs et al.

Re claims 9 and 17, Dove et al. and Yasumura et al. disclose in claims 6 and 12 respectively above,

Dove et al. and Yasumura et al. do not disclose

a second dielectric layer located over the other dielectric layer; and wherein the electrical feedthroughs include conducting paths located on the second dielectric layer,

However, Dove et al. disclose

three conductive layer (145) and two dielectric layers (150) stacked together (fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add another dielectric layer and conductive layer in the device of Dove et al. as a second dielectric layer and a conductive path, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Dove et al. and Yasumura et al. do not disclose

the conducting paths being physically connecting by metal-filled vias to the portions of the electrical feedthroughs in the trenches.

Jacobs et al. teaches a device wherein

the conducting paths being physically connecting by metal-filled vias (metal filled via [col. 8, line 39]) to the portions of the electrical feedthroughs in the trenches.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use the metal-filled vias as taught by Jacobs et al. in the device of Dove et al. et al., in order to make the wiring path between two conductive layers electrically continuous. (Jacobs et al. col., col. 8, line 40]).

Re claim 13, Dove et al. and Yasumura et al. disclose

The method of claim 12,

Dove et al. and Yasumura et al. do not disclose,

the forming electrical feedthroughs produces a density of at least 10 of said feedthroughs per millimeter along part of the joint.

Jacobs et al. teaches a device including

the forming electrical feedthroughs produces a density of at least 10 of said feedthroughs per millimeter along part of the joint. (having very high wiring density (i.e. 5 micron lines on a 10 micron pitch) [col. 9, line 10])

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replacing the electrical feedthroughs of Dove et al. with higher density feedthroughs as taught by Jacobs et al., “to provide an integrated circuit packaging structure which can provide the high circuit density, high speed characteristics of wafer scale integration while high manufacturing yields are possible.” (Jacobs et al., [col. 4, line 23])

7. Claims 10, 11, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dove et al. in view of Yasumura et al. as applied to claims 6-8, 12, 15, 16, and 20 above and further in view of Tatum et al. (US20040076205).

Re claims 10, 11, 18 and 19, Dove et al. and Yasumura et al. disclose in the claims 6 and 12 respectively above,

Dove et al. and Yasumura et al. do not disclose

the micro-electronic structure including a two-dimensional array of MEMS devices, VCSELs, or sensors,

the micro-electronic structure including a 2D array of MEMS-controlled optical elements and the housing comprising a window capable of passing infrared or visible light.

Tatum et al. teaches a device wherein

the micro-electronic structure includes a two-dimensional array (a two-dimension array [0069]) of MEMS devices (use MEMs (micro-electro-mechanical-structures [0005]), VCSELs, or sensors,

the micro-electronic structure includes a 2D array (a two-dimension array [0069]) of MEMS-controlled optical elements (use MEMs (micro-electro-mechanical-structures [0005]) and the housing comprises a window (a housing window [0028]) capable of passing infrared or visible light.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add a two-dimensional array MEMs and a housing window as taught by Tatum et al. in the electrical device of Dove et al.,

in order to be able to tune the resonating wavelength of the coherent photonic emission for such VCSELs. (Tatum, paragraph [0005])

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dove et al. in view of Yasumura et al. and Tatum et al. as applied to claim 13 above, and further in view of Steddom et al.

Re claim 14, Dove et al. show and disclose

The method of claim 13,

Dove et al., Yasumura et al. and Tatum et al. do not disclose

wherein the metallic electrical feedthroughs have heights normal to the top surface of at least 0.5 micro-meters.

Steddom et al. teaches a device wherein

the metallic electrical feedthroughs have heights (integrating transmission lines (feedthroughs) have a thickness about 5 to about 50 microns [0041]) normal to the top surface of at least 0.5 micro-meters.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to replacing the electrical feedthroughs of Dove et al. et al. with same thickness as taught by Jacobs et al., in order to meet the requirements for good impedance control and low insertion loss at high frequencies that reach 100 GHz and higher (Dive et al. paragraph [0041]).

10) Response to Arguments

Appellant's arguments filed 3-06-09 have been fully considered but they are not persuasive.

1) **Claims 1 and 3**,

a) Appellant argues that Dove in view of Yasumura and Jacobs does not teach all of the elements of Claim 1;

This argument is not persuasive because

(1) Dove in view of Yasumura and Jacobs teaches all the limitations in Claim 1, as the examiner cited in the final rejection.

(2) The argument of the conductive layer and the micro-element structure used same reference number 145 is right, but it is a typographic error in the final rejection; Since the micro-element structure is an integrated chip (same as in the application) is clearly shown in the fig. 1, which the examiner used in the rejection, and the micro-element structure (110, fig. 1) is shown connecting the conductive layer (145, fig. 1), therefore, the reference number 145 used for both of the conductive layer and the micro-element structure was an obvious typographic error, and the reference number for the micro-element structure should be 110, fig. 1.

b) Appellant argues that Dove in view of Yasumura is not a proper combination that (A) Dove teaches away from the presence of Yasumura's channel, (B) There is no reasonable expectation of success of introducing Yasumura's electrical interconnections into Dove's apparatus, and (C) No articulated reasoning with rational underpinnings to support the combination of Dove in view of Yasumura.

This argument is not persuasive because

(A) The statement of Dove (C. 2, L.13-22) cited by applicant, of which, Dove is used in the background of the invention, and which is unrelated to the modification at all. The Figures used in the argument are not used in the rejection and are not related the rejection.

Since the feedthrough of Yasumura is constructed horizontally (fig. 46), and the feedthrough is parallel to the conductive layers and it would not break any of the conductive layers.

(B) Dove disclose the conductive lead, (Dove's lead is on the surface of the board), Yasumura teaches a feedthrough structure, a channel with a conductive lead, (cut out a channel in the board and place the conductive lead in the channel), therefore, using Yasumura's feedthrough structure in Dove's device is performable and reasonable.

(C) As in the final rejection, examiner clearly stated the motivation to combine the reference of Dove and Yasumura: in order to reduce the size and increase the stability and integrity of structure of the device, and a person having ordinary skill in the art would recognize the motivation easily, since the modification integrating the conductors into the channels of the substrate instead of the conductors laying on the surface of the substrate is well known in the electronic housing art.

2) **Claims 2 and 4**,

Appellant argues that "One problem attendant with the more traditional method of sealing the metal cover to the cavity uses conductive epoxy" and Dove does not teach or suggest a hermetically sealed cavity.

This arguments is not persuasive because

a) Again, as pointed out above, applicant using the background of the invention of Dove, which is not related and was not used in the rejection at all.

b) Dove clearly disclose wherein the joint, housing, and substrate hermetically seal the cavity (the metal cover is sealed to the cavity [col. 1, line 43]), and shows in figure 1.

3) **Claim 5**

Appellant argues that there is no motivation to combine the teaching of Tatum with Dove, Yasumura, Jacob, and Steddom.

This arguments is not persuasive because

a) The teaching of Tatum does not related to any modification of the device of Dove by Yasumura, Jacob, or Steddom.

b) The motivation is clearly stated in the final rejection that it would have been obvious to one having ordinary skill in the art at the time the invention was made to add the optical device and a window as taught by Tatum et al. in the housing of the electrical device of Dove et al. et al., in order to be able to couple the device to the faster optical communications applications (Tatum et al. paragraph [0002]).

4) **Claims 6-8, 12, 15-16, and 20**

The argument is not persuasive because Applicant repeated the arguments in claim 1 above.

5) **Claims 9, 13, and 17**

No specific argument besides the dependence of the claim and the arguments in response of the arguments regarding claims 6 and 12 above.

6) **Claims 10-11 and 18-19**

No specific argument besides the dependence of the claim and the arguments in response of the arguments regarding claims 6 and 12 above.

6) **Claim 14**

No specific argument besides the dependence of the claim and the arguments in response of the arguments regarding claim 12 above.

11) Related proceedings appendix

No decision rendered by a court or the board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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