IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Atsushi KUWATA

Serial No.:	11/372,198	Group Art Unit:	2186
Filed:	March 10, 2006	Examiner:	Dudek

For: DISK ARRAY DEVICE AND SHARED MEMORY DEVICE THEREOF, AND CONTROL PROGRAM AND CONTROL METHOD OF DISK ARRAY DEVICE

Commissioner of Patents
Alexandria, VA 22313-1450

APPELLANT'S REPLY BRIEF ON APPEAL

Sir:

Based on the new arguments and comments made of record by the Examiner for the first time during prosecution, Appellant respectfully submits the following reply to the Examiner's Answer mailed on September 30, 2009.

I. The rejection of record fails to establish a *prima facie* obviousness rejection by failing to demonstrate all elements of the claimed invention, based on primary reference Fujimoto

The claimed invention describes both structure and function in all of the independent claims. Therefore, the prior art evaluation must start out by assuming both the structure and function of the cited primary reference.

Appellant has repeatedly requested during prosecution that the Examiner take into account the structure of primary reference Fujimoto and then identify the

differences and provide a reasonable rationale to modify the structure that is demonstrated in Fujimoto to arrive at the structure of the claimed invention.

The evaluation of record does not follow this fundamental obviousness evaluation and, therefore, fails to provide a *prima facie* obviousness rejection.

Instead, the evaluation of record accounts only for functional similarities but ignores the structure of primary reference Fujimoto.

II. The following technical analysis based on primary reference Fujimoto clearly demonstrates that the Examiner has erred in the prior art evaluation

II(a). The structure clearly described by independent claim 1 requires a director device that manages the I/O of data from an external device and the disk drive device, where the director device has a command control unit that transmits the command for controlling of a cache memory and that receives a processing result.

The only structure in primary reference Fujimoto that would seem to reasonably satisfy this structural/functional description is shown in Figure 7 and would have to be the "Host IF" 102 that corresponds to the "director device" of the claim, and that includes microprocessor 101 that would have to correspond to the "command control unit" of the claim (e.g., see lines 6-9 of column 7).

II(b). Claim 1 also clearly describes a "shared memory device having a cache memory" and having a "processing unit" that executes control of the cache memory and that has a "command control unit" that receives commands from the director device's command control unit, and that transmits the processing result back to the command control unit.

The only structure in primary reference Fujimoto that would seem to reasonably satisfy this structural/functional description is shown in Figure 7 and would have to be the "Cache Memory Unit" 14 described as having a cache memory 109 and controller 108 (e.g., see lines 43-45 of column 7).

II(c). The final claim limitation of claim 1 also clearly describes that a serial bus interconnects the command control unit of the director device with the command control unit of the shared memory device.

There clearly is no serial bus interconnecting microprocessor 101 with CM controller 108 in Figure 7 of Fujimoto. Therefore, the Examiner has the initial burden of providing a reasonable rationale (e.g., one of the seven rationales set out in KSR) to modify the structure shown in Figure 7 of Fujimoto to incorporate a serial data bus between microprocessor 101 and CM controller 108.

The closest attempt in the rejection of record that attempts to address this aspect of the claimed invention the Examiner's new argument, presented for the first time in the Examiner's Answer in paragraph (10) on page 17:

"*The specific type of bus is not disclosed by Fujimoto, however, there are two types of busses that [exist] for this purpose, parallel or serial. Each bus has its own advantages, and it would have been obvious to try each of these busses, since there are a limited number of choices, in an attempt to solve the problem of connecting these devices together. Furthermore, when the combination of Fujimoto and Millard is made there would be additional processors for the shared memory devices. This would result in an interconnection of multiple processors, which Millard disclosed can be done with a serial bus (see column 2, line 60).*"

Appellant submits that there are at least three problems with the Examiner's new argument recited above and that this rationale is insufficient to demonstrate obviousness.

First, as explained in paragraph [0009] of the disclosure of the present application, the conventional wisdom for interconnecting two processors used for disk array devices is by way of using a shared bus. In contrast, the final limitation of the claimed invention explicitly requires that a serial communication bus be used for transmission of commands and processing results. All of the references of record, including primary reference Fujimoto, appear to follow this conventional architecture of using a shared bus.

Thus, contrary to the conventional wisdom in the art at the time of the invention, the claimed invention modifies the conventional architecture by separating

the bus functions between processors by providing a high speed serial bus dedicated to commands/processing results.

Neither Fujimoto nor Millard suggests separating bus functions in the manner described by the claimed invention. That is, neither reference suggests using a serial command bus in combination with the conventional shared bus that would remain to provide parallel data transmission between processors in a disk array device.

Therefore, even if Millard were considered to be properly combinable with Fujimoto, there would still be no suggestion of providing a dedicated a high speed serial bus specifically for purpose of transmitting commands and returned processing results. The claimed invention separates the transmission paths of data and commands, and uses a high speed serial bus specifically for the command bus, which is not taught or suggested in either cited reference.

Thus, the combination of the claimed invention is more than merely trying a serial bus as a shared bus versus using a parallel bus as the shared bus, as the Examiner alleges in his new argument. Indeed, using a serial bus to replace a parallel bus that is a shared bus would only slow down the overall shared bus transmission, absent some type of objective evidence by the Examiner, which evidence is not currently of record.

Second, as Appellant has repeatedly pointed out during prosecution, the details of the architecture of secondary reference demonstrate a completely different principle of operation from that of primary reference Fujimoto. It is, therefore, not properly combinable under the holding of *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), as described in MPEP 2143.01: "*If the proposed modification or combination would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious.*"

That is, the extraction of specific design features from two circuits operating under two fundamentally different principles of operation is clear indication of impermissible hindsight, unless the Examiner demonstrates that the extracted feature is reasonably either a direct substitution performing the identical function in both circuits or provides an improvement in the context of the circuit of the primary reference. In the final sentence on page 4 of the Examiner's Answer, the Examiner himself

characterizes secondary reference Millard as demonstrating a fundamentally different approach (*e.g.*, different principle of operation) from that of primary reference Fujimoto.

Stated slightly differently in the concepts of *KSR*, since circuits do not function as abstract ideas that can be freely rearranged based upon a roadmap of a claimed invention, extracting a design detail from two references having drastically different architectural details, even if both circuits arguably perform similar functions, would clearly violate the requirement of *KSR* that the Examiner demonstrate an expectation of success, since the primary reference already performs the similar function without any improvement or substitution of an element of a system having a drastically different configuration. Therefore, the modification of primary reference Fujimoto by Millard is improper in the rejection of record, since there is no reasonable motivation to modify the primary reference and no expectation of success absent impermissible hindsight.

Third, the description involving line 60 of column 2 of Millard, upon which the Examiner relies in the rejection of record, actually recites:

"*The communications level processor is configured to communicate with a host computer, an intelligent terminal or other processor devices on either a serial, parallel or DMA basis and performs all communications functions with such external devices, such as handshake, protocol and the like.*"

Appellant submits that the above-recited description makes no suggestion to incorporate a serial communication bus explicitly for purpose of transmitting commands and receiving processing results, and the most that can reasonably be concluded from the Examiner's new argument is that the Examiner concludes that the claimed invention would have been possible at the time of the invention.

The Examiner's allegation that "... *it would have obvious to try each of these busses, since there are a limited number of choices, in an attempt to solve the problem of connecting these devices together*" is not supported by objective evidence and does not arrive at the claimed invention, since it is specifically the command bus between two specific processors that is described as using the serial communication bus.

That is, the claimed invention involves more than "merely trying different buses", since it also includes separating the commands/responses from a shared bus

between two specific processors in a disk array device, and incorporating, instead, a serial bus dedicated to commands/responses, as well as using the conventional parallel data bus for the data between these two processors.

Stated slightly differently, if the Examiner's allegation were correct that it would be "obvious to try each of different busses", then there would clearly be no burden on the Examiner to demonstrate, by objective evidence, at least one example of such configuration described in the independent claims. The failure to provide any objective evidence is clear indication of improper hindsight.

Thus, the Examiner's newly-articulated reliance on "obvious to try" is clearly misplaced, since the Appellant's own evaluation above demonstrates that the element missing from primary reference Fujimoto is more than a mere substitution of allegedlly "obvious to try" alternatives.

That is, rather than merely "trying" a serial bus rather than a parallel bus, a key difference between the claimed invention and primary reference Fujimoto is that the shared bus of the conventional architectural wisdom is modified to provide a high speed serial bus dedicated to transporting command/process reports between two of the processors in a disk array device. None of the references of record demonstrate this claim element, and the rejection of record fails to properly identify this difference.

III. The evaluation of record fails to comply with the requirements set forth in *KSR* describing that the Examiner has the initial burden to identify the differences from the primary reference (*i.e.*, Fujimoto) and then provide an articulation of a reasonable rationale to modify that primary reference to arrive at the claimed invention

That is, in ignoring the structure described in the claimed invention, the rejection of record has also failed to properly recognize the differences between primary reference Fujimoto and the claimed invention, since the claimed invention involves more than the mere replacement of the shared bus demonstrated in the prior art references. Rather, the claimed invention actually describes two processors in a disk array device having a bus dedicated to commands and process reports.

The Examiner's new argument based on "obvious to try" is misplaced, since the difference between Fujimoto and the independent claims is not a simple substitution of

a limited number of known alternatives. Rather, the claimed invention involves a modification to the shared bus conventionally used in disk array devices.

CONCLUSION

In view of the foregoing, Appellant submits that the Examiner has clearly erred in the rejections currently of record and that claims 1, 3-17, and 19-31, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. Thus, the Board is respectfully requested to reverse all rejections of claims 1, 3-17, and 19-31.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Attorney's Deposit Account number 50-0481.

Respectfully submitted,

Dated: 11/30/09

Frederick E. Cooperrider
Reg. No. 36,769

McGinn Property Law Group, PLLC
8231 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer Number: 21254

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ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
- ☐ Fee Attached
- ☐ Amendment / Reply
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
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Firm Name	McGinn Intellectual Property Law Group, PLLC 8321 Old Courthouse Road, Suite 200, Vienna, Virginia 22182		
Signature			
Printed name	Frederick E. Cooperrider, Esq.		
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