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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ATSUSHI KUWATA

Appeal 2010-003807
Application 11/372,198
Technology Center 2100

Before HOWARD B. BLANKENSHIP, THU A. DANG, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

DANG, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a Final Rejection of claims 1, 3-17, and 19-31. Claims 2 and 18 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

A. INVENTION

According to Appellant, the invention relates to a disk array device using a high-speed throughput bus and a shared memory device thereof, a control program and a control method of the disk array device (Spec. 1, ll. 6-12).

B. ILLUSTRATIVE CLAIM

Claim 1 is exemplary:

1. A disk array device, comprising:

a director device which manages input/output of data to/from an external device and a disk drive device; and

a shared memory device having a cache memory for input/output data,

wherein said director device transmits a command for instructing on control of the cache memory for said input/output data to said shared memory device, and said shared memory device executes control of said cache memory for said input/output data based on a command from said director device,

wherein said director device includes:

a command control unit which transmits said command and receives a processing result for said command which is sent from said shared memory device,

wherein said shared memory device includes:

a processing unit which executes control of said cache memory for said input/output data based on a command from said director device, and

> a command control unit which receives a command from said director device and transmits a processing result for said command from said shared memory device, and
>
> wherein the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus.

C. REJECTION

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Millard	US 4,096,567	Jun. 20, 1978
Scaringella	US 6,467,047 B1	Oct. 15, 2002
Fujimoto	US 6,477,619 B1	Nov. 05, 2002

Claims 1, 3-13, 16, 17, 19-22, and 25-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto and Millard.

Claims 14, 15, 23, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto, Millard and Scaringella.

II. ISSUE

The dispositive issue before us is whether the Examiner has erred in concluding that Fujimoto in view of Millard would have suggested a "director device" that includes "a command control unit which transmits said command and receives a processing result for said command which is sent from said shared memory device" and a "shared memory device" which includes "a command control unit which receives a command from said

director device and transmits a processing result for said command" wherein "the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus" (claim 1). In particular, the issue turns on whether Fujimoto in view of Millard would have suggested a serial communication bus connecting a command control unit of a director device and a command control unit of a shared memory device.

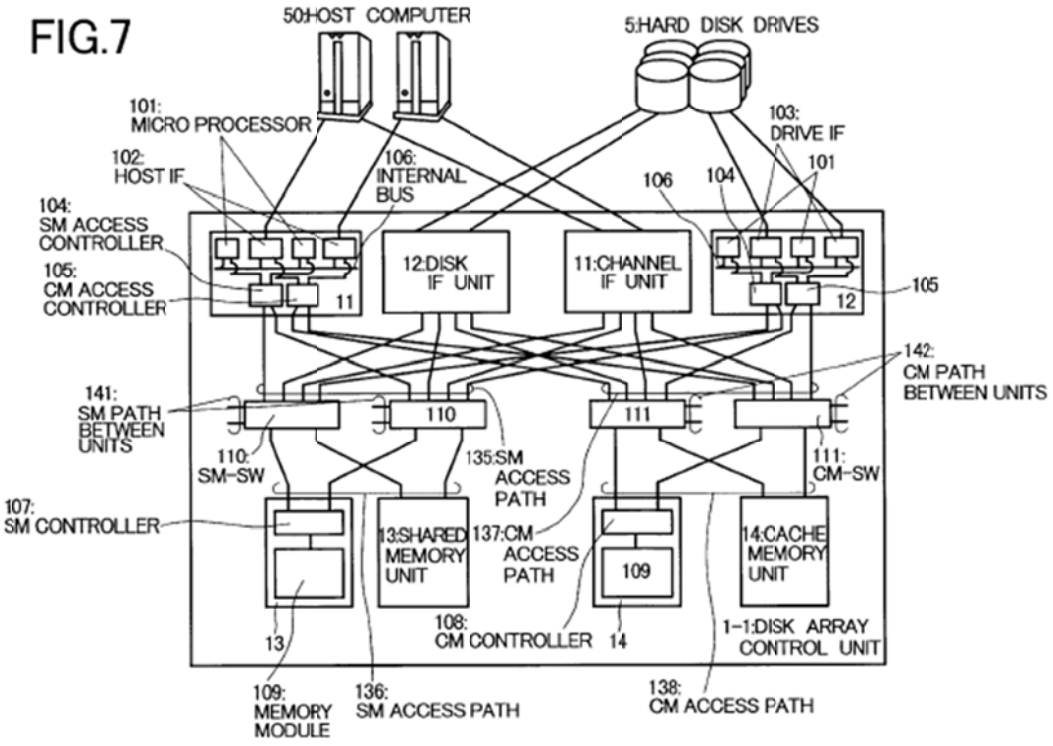
III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Fujimoto

1. Fujimoto discloses a disk array controller 1 that includes channel interface (IF) units 11 for interfacing with host computers 50, disk IF units 12 for interfacing with hard disk drives 5, shared memory units 13, and cache memory units 14; wherein, the channel IF units 11, disk IF units 12, and the shared memory units 13 are connected by an interconnection 210 and the cache memory units 14 are connected by another interconnection 220 (col. 6, ll. 42-56; Figs. 7 and 8).

2. Fujimoto's Fig. 7 is reproduced below:



Fujimoto's Fig. 7 discloses a channel IF unit 11 that includes two microprocessors 101 for controlling the data transaction with the host computers 50, an SM access controller 104 for controlling the access to the shared memory units 13, and a CM access controller 105 for controlling the access to the cache memory units 14 (col. 7, ll. 6-15).

3. As shown in Fig. 7, the cache memory unit 14 includes a cache memory (CM) controller 108 and a memory module 109, and temporarily stores data to be recorded (col. 7, ll. 43-46).

4. The microprocessors 101 and host IFs 102 are connected by an internal bus 106, and the CM access controller 105 is connected directly to the two hosts IFs 102 (col. 7, ll. 15-18), while the CM access controller 105

is connected to the two CM-SWs 111 by two CM access paths 137, and the CM-SWs 111 are connected to the two CM controllers 108 by two access paths 138, enabling each CM controller 105 to have two access routes to each CM controller 108 (col. 7, ll. 58-64).

Millard

5. Millard's Fig. 1 is reproduced below:

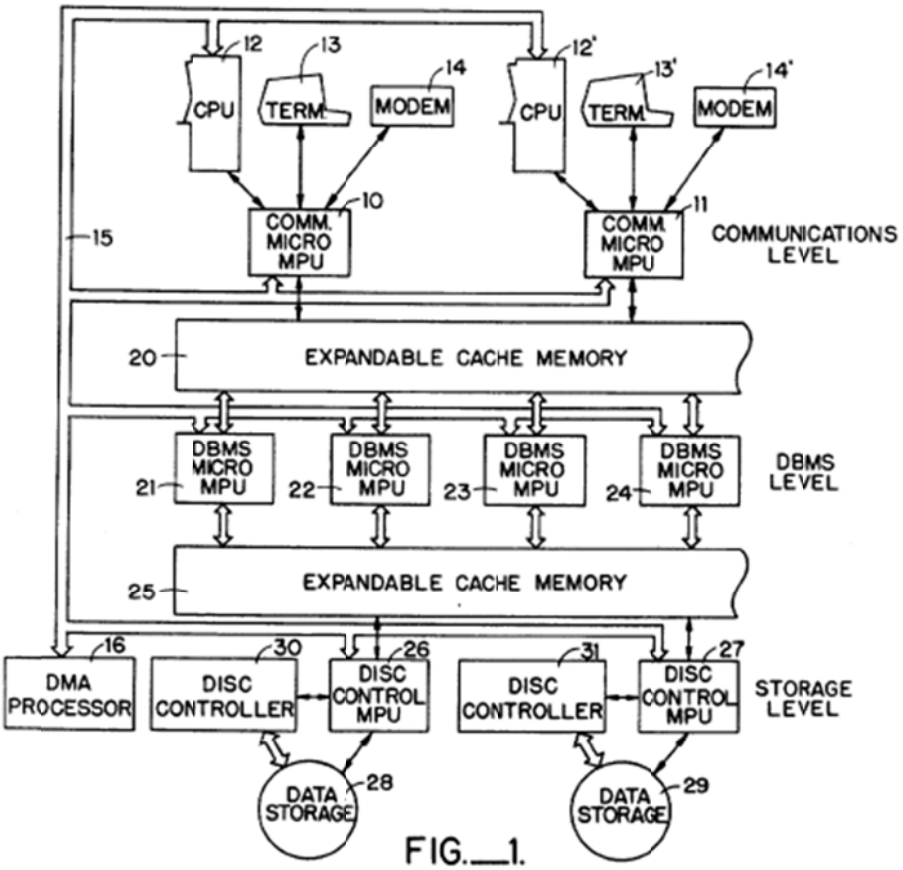


FIG. 1.

Millard's Fig. 1 discloses an information storage facility with multiple level processors wherein a direct memory access bus is provided which enables high speed data transfer among the several processors included within the storage facility and also external host computers or intelligent terminals (Abstract).

6. The communications level processor is configured to communicate with a host computer, an intelligent terminal or other processor devices on a serial, parallel or DMA basis and performs all communication functions with such external devices (col. 2, ll. 57-63).

IV. ANALYSIS

Claims 1, 3-13, 16, 17, 19-22, and 25-31

Appellant contends that "there is no demonstration [in the cited references] of: '… wherein the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus', as required by independent claim 1" (App. Br. 11). In particular, Appellant contends that "neither Fujimoto nor Millard has the structural components described in even the independent claims, including the two command control units, let alone a high speed serial bus interconnecting these two components" (App. Br. 12). Appellant then contends that "Fujimoto does not have its two interfaces (e.g., the channel IF unit 11 and the disk IF unit 12) controlled by a single entity such as the director device of the claimed invention" and thus Fujimoto and Millard's "architectures are distinctly different from each other and from the claimed invention" (App. Br. 13).

However, the Examiner finds that "Fujimoto consists of disk array controllers that are all interconnected to each other and function to control access to disk drives from host computers" (Ans. 18). In particular, the Examiner finds that "Fujimoto describes the connections between all the components of the system" and notes that though "[t]he specific type of bus is not disclosed by Fujimoto . . . , there are two types of busses that

exist[s](sic) for this purpose, parallel or serial" (Ans. 17*)*. The Examiner then concludes that "when the combination of Fujimoto and Millard is made there would be additional processors for the shared memory devices" and notes that such combination "would result in an interconnection of multiple processors, which Millard disclosed can be done with a serial bus" (Ans. 18).

Though in the Reply Brief, Appellant admits that "'Host IF' 102 [of Fujimoto] corresponds to the 'director device' of the claim," that "microprocessor 101 [of Fujimoto] would have to correspond to the 'command control unit' of the claim," and that "'shared memory device having a cache memory' . . . . would have to be the 'Cache Memory Unit' 14 described as having a cache memory 109 and controller 108" (Reply Br. 2), Appellant argues that "[t]here clearly is no serial bus interconnecting microprocessor 101 with CM controller 108" in Fujimoto (Reply Br. 3). Appellant contends that "the conventional wisdom for interconnecting two processors used for disk array devices is by way of using a shared bus" (Reply Br. 3). Thus, Appellant contends that "even if Millard were properly combinable with Fujimoto, there would still be no suggestion of providing a dedicated … high speed serial bus specifically for [the] purpose of transmitting commands and returned processing results" (Reply Br. 4 (emphasis omitted)).

Appellant's arguments that "Fujimoto does not have its two interfaces … controlled by a single entity" (App. Br. 13) and that there are "no suggestion of providing a dedicated … high speed serial bus specifically for [the] purpose of transmitting commands and returned processing results" (Reply Br. 4 (emphasis omitted)) are not commensurate in scope with the

recited language of claim 1. That is, claim 1 does not require a "single" entity controlling two interfaces or any bus "specifically for purpose of transmitting commands and returned processing results" as Appellant contends. Rather, claim 1 merely requires that the command control unit of the director device is connected to the command control unit of the shared memory device by a "serial communication bus." Further, since claim 1 does not define as to what a "director device" is to mean, include or represent, contrary to Appellant's argument (App. Br. 13), claim 1 does not preclude a "director device" that comprises a plurality of separate interfaces that perform separate functions. Accordingly, in this Appeal, we address whether the teachings of Fujimoto in view of Millard would have suggested a serial communication bus connecting a command control unit of a director device and a command control unit of a shared memory device, as specially required by claim 1.

Fujimoto discloses a disk array device comprising interfaces that manage input/output of data to/from an external device and a disk drive device (FF 1) and shared memory units including a cache memory for input/output data (FF 3), wherein the interfaces comprise microprocessors for controlling the data transaction with the shared memory units and the cache memory comprises a cache memory controller and a memory module (FF 2-3). We find Fujimoto's interfaces to comprise "a director device which manages input/output data to/from an external device and a disk drive device" and find Fujimoto's microprocessor of the interfaces as "a command control unit which transmits said command and receives a processing result" as recited in claim 1. We also find Fujimoto's shared memory units to comprise "a shared memory device having a cache memory for input/output

data" wherein the cache memory controller comprises "a processing unit which executes control of said cache memory" and "a command control unit which receives a command from said director device" as recited in claim 1. In fact, even Appellant admits that "'Host IF' 102 [of Fujimoto] corresponds to the 'director device' of the claim," that "microprocessor 101 [of Fujimoto] would have to correspond to the 'command control unit' of the claim," and that "'shared memory device having a cache memory' . . . . would have to be the 'Cache Memory Unit' 14 described as having a cache memory 109 and controller 108" (Reply Br. 2).

Furthermore, Fujimoto discloses that microprocessor 101 and host IF 102 are connected, whereby CM access controller 105 is connected to host IF 102 (FF 4). We find microprocessor 101 to be connected to CM access controller 105. Furthermore, CM access controller 105 is also connected to CM controller 108 (*id*). Accordingly, we find microprocessor 101 to be connected to CM controller 108 via CM access controller 105. Thus, we find Fujimoto discloses that the command control unit of a director device is connected to the command control unit of the shared memory device as required by claim 1.

We thus agree with the Examiner's finding that "Fujimoto describes the connections between all the components of the system" (Ans. 17). Further, we find no error with the Examiner's finding that, though "[t]he specific type of bus is not disclosed by Fujimoto . . . , there are two types of busses that exists for this purpose, parallel or serial" (Ans. 17). In fact, as Millard discloses, communications between processors, a host computer, an intelligent terminal or other processor devices may be on a serial or parallel basis (FF 6). That is, Millard discloses the use of direct communication bus

(serial or parallel) to enable high speed data transfer among the several processors included within the storage facility and also external host computers or intelligent terminals (FF 5-6).

Accordingly, we find no error in the Examiner's conclusion that Fujimoto in view of Millard would have suggested a serial communication bus connecting a command control unit of a director device and a command control unit of a shared memory device as required by claim 1. That is, contrary to Appellant's contention (App. Br. 12), we conclude that Fujimoto in view of Millard do at least suggest two command control units, wherein "a high speed serial bus interconnecting these two components" (App Br. 12) is provided therebetween.

Although Appellant also argues that, because "architectures are distinctly different from each other and from the claimed invention," the prior art teachings "preclude a conclusion of obviousness" (App. Br. 13), Appellant appears to have viewed the references from a different perspective than the Examiner. The issue here is not whether the ordinarily skilled artisan would have added Millard's system with Fujimoto's system but whether the artisan, upon reading Millard, would find it obvious to use a serial bus for high speed data transfer as the communication bus of Fujimoto. The Supreme Court has determined that the conclusion of obviousness can be based on the interrelated teachings of multiple patents, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

Here, both Fujimoto and Millard are directed to the same field of endeavor of cache memory control. We conclude that such application of Millard's serial bus for high speed data transfer as the bus for data transfer in Fujimoto is no more than a simple arrangement of old elements with each performing the same function it had been known to perform, yielding no more than one would expect from such an arrangement. *KSR*, 550 U.S. at 416. The skilled artisan would "be able to fit the teachings of multiple patents together like pieces of a puzzle" since the skilled artisan is "a person of ordinary creativity, not an automaton." *Id*. at 420-21. As stated by the Supreme Court, an obviousness "analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id*. at 418. *See also Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006).

Accordingly, we find that the Examiner did not err in rejecting independent claim 1 over Fujimoto in view of Millard.

As for independent claims 17, 26, and 29, Appellant merely repeats the claim language (App. Br. 16) but does not provide arguments separate from those of claim 1 (App. Br. 17-18). As discussed above with respect to claim 1 which recites similar features, we conclude that Fujimoto in view of Millard would have suggested the recited features. As a result, we find that the Examiner also did not err in rejecting independent claims 17, 26 and 29 over Fujimoto in view of Millard. Appellant does not provide arguments for claims 3-13, 16, 19-22, and 25, 27, 28, 30 and 31 separate from those of claims 1, 17, 26, and 29 from which they respectively depend, other than to

say "there are no corresponding configurations in the cited references, as required by claims 7-13" (App. Br. 18). Accordingly, claims 3-13, 16, 19-22, and 25, 27, 28, 30 and 31 fall with claims 1, 17, 26, and 29.

Claims 14, 15, 23, and 24

As for claims 14, 15, 23, and 24, Appellant merely contend that "these claims are allowable for at least the same reasons that their underlying base claims are allowable as set forth above" (App. Br. 18). As discussed above with respect to claims 1 and 17 from which claims 14, 15, 23 and 24 respectively depend, we find no error in the Examiner's rejection of the claims over Fujimoto in view of Millard. Accordingly, we find that the Examiner also did not err in rejecting independent claims 14, 15, 23 and 24 over Fujimoto and Millard in further view of Scaringella.

V. CONCLUSION AND DECISION

The Examiner's rejection of claims 1, 3-17, and 19-31 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

peb