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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/372,198	03/10/2006	Atsushi Kuwata	MA-674-US	4344

21254 7590 01/12/2012

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EXAMINER	
DUDEK JR, EDWARD J	

ART UNIT	PAPER NUMBER
2186	

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ATSUSHI KUWATA

Appeal 2010-003807
Application 11/372,198
Technology Center 2100

Before HOWARD B. BLANKENSHIP, THU A. DANG, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

DANG, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a Final Rejection of claims 1, 3-17, and 19-31. Claims 2 and 18 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

A. INVENTION

According to Appellant, the invention relates to a disk array device using a high-speed throughput bus and a shared memory device thereof, a control program and a control method of the disk array device (Spec. 1, ll. 6-12).

B. ILLUSTRATIVE CLAIM

Claim 1 is exemplary:

1. A disk array device, comprising:

a director device which manages input/output of data to/from an external device and a disk drive device; and

a shared memory device having a cache memory for input/output data,

wherein said director device transmits a command for instructing on control of the cache memory for said input/output data to said shared memory device, and said shared memory device executes control of said cache memory for said input/output data based on a command from said director device,

wherein said director device includes:

a command control unit which transmits said command and receives a processing result for said command which is sent from said shared memory device,

wherein said shared memory device includes:

a processing unit which executes control of said cache memory for said input/output data based on a command from said director device, and

> a command control unit which receives a command from said director device and transmits a processing result for said command from said shared memory device, and
>
> wherein the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus.

C. REJECTION

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Millard	US 4,096,567	Jun. 20, 1978
Scaringella	US 6,467,047 B1	Oct. 15, 2002
Fujimoto	US 6,477,619 B1	Nov. 05, 2002

Claims 1, 3-13, 16, 17, 19-22, and 25-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto and Millard.

Claims 14, 15, 23, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto, Millard and Scaringella.

II. ISSUE

The dispositive issue before us is whether the Examiner has erred in concluding that Fujimoto in view of Millard would have suggested a "director device" that includes "a command control unit which transmits said command and receives a processing result for said command which is sent from said shared memory device" and a "shared memory device" which includes "a command control unit which receives a command from said

director device and transmits a processing result for said command" wherein "the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus" (claim 1). In particular, the issue turns on whether Fujimoto in view of Millard would have suggested a serial communication bus connecting a command control unit of a director device and a command control unit of a shared memory device.

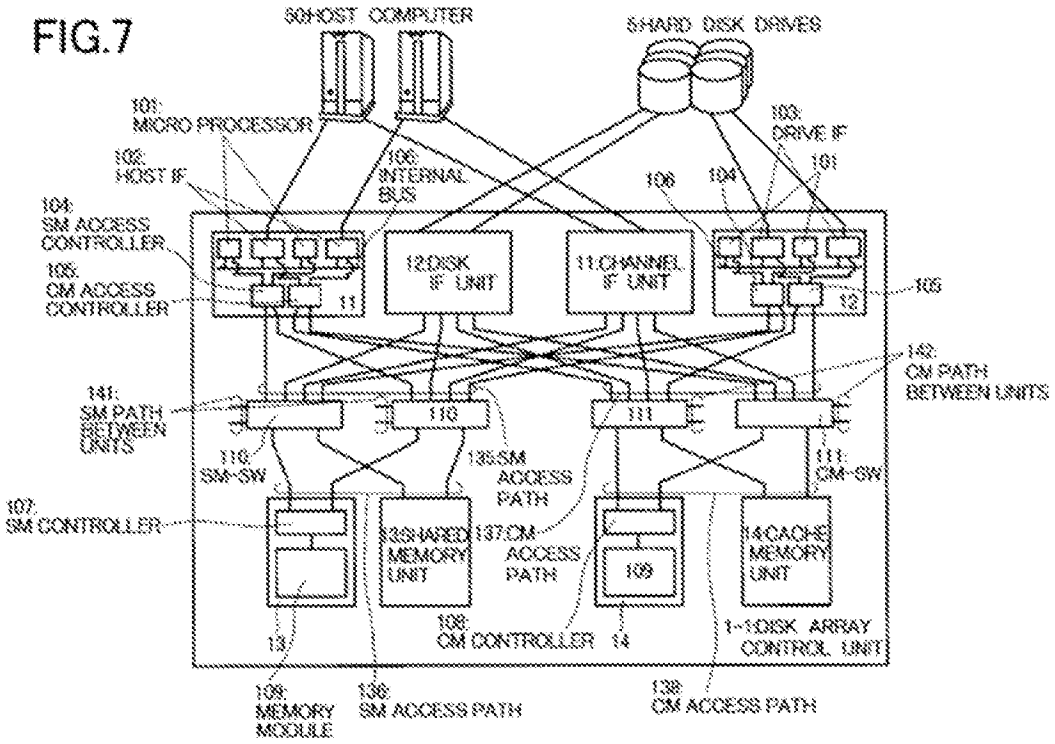
III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Fujimoto

1. Fujimoto discloses a disk array controller 1 that includes channel interface (IF) units 11 for interfacing with host computers 50, disk IF units 12 for interfacing with hard disk drives 5, shared memory units 13, and cache memory units 14; wherein, the channel IF units 11, disk IF units 12, and the shared memory units 13 are connected by an interconnection 210 and the cache memory units 14 are connected by another interconnection 220 (col. 6, ll. 42-56; Figs. 7 and 8).

2. Fujimoto's Fig. 7 is reproduced below:



Fujimoto's Fig. 7 discloses a channel IF unit 11 that includes two microprocessors 101 for controlling the data transaction with the host computers 50, an SM access controller 104 for controlling the access to the shared memory units 13, and a CM access controller 105 for controlling the access to the cache memory units 14 (col. 7, ll. 6-15).

3. As shown in Fig. 7, the cache memory unit 14 includes a cache memory (CM) controller 108 and a memory module 109, and temporarily stores data to be recorded (col. 7, ll. 43-46).

4. The microprocessors 101 and host IFs 102 are connected by an internal bus 106, and the CM access controller 105 is connected directly to the two hosts IFs 102 (col. 7, ll. 15-18), while the CM access controller 105

is connected to the two CM-SWs 111 by two CM access paths 137, and the CM-SWs 111 are connected to the two CM controllers 108 by two access paths 138, enabling each CM controller 105 to have two access routes to each CM controller 108 (col. 7, ll. 58-64).

Millard

5. Millard's Fig. 1 is reproduced below:

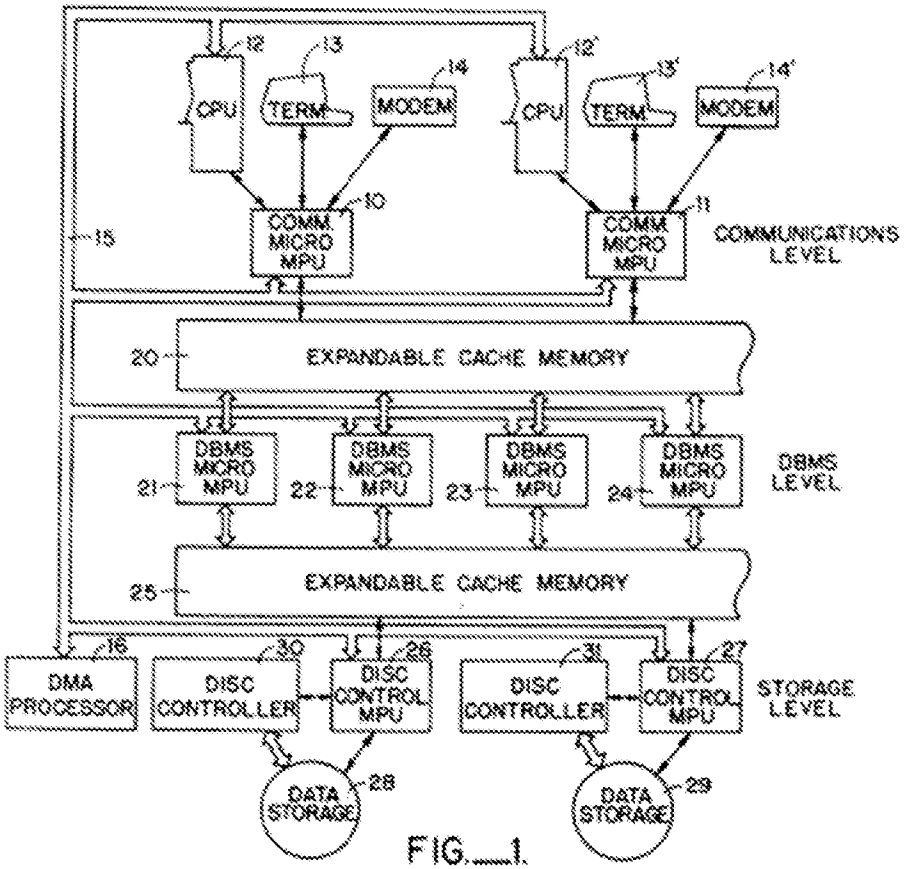


FIG. 1.

Millard's Fig. 1 discloses an information storage facility with multiple level processors wherein a direct memory access bus is provided which enables high speed data transfer among the several processors included within the storage facility and also external host computers or intelligent terminals (Abstract).

6. The communications level processor is configured to communicate with a host computer, an intelligent terminal or other processor devices on a serial, parallel or DMA basis and performs all communication functions with such external devices (col. 2, ll. 57-63).

IV. ANALYSIS

Claims 1, 3-13, 16, 17, 19-22, and 25-31

Appellant contends that "there is no demonstration [in the cited references] of: '… wherein the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus', as required by independent claim 1" (App. Br. 11). In particular, Appellant contends that "neither Fujimoto nor Millard has the structural components described in even the independent claims, including the two command control units, let alone a high speed serial bus interconnecting these two components" (App. Br. 12). Appellant then contends that "Fujimoto does not have its two interfaces (e.g., the channel IF unit 11 and the disk IF unit 12) controlled by a single entity such as the director device of the claimed invention" and thus Fujimoto and Millard's "architectures are distinctly different from each other and from the claimed invention" (App. Br. 13).

However, the Examiner finds that "Fujimoto consists of disk array controllers that are all interconnected to each other and function to control access to disk drives from host computers" (Ans. 18). In particular, the Examiner finds that "Fujimoto describes the connections between all the components of the system" and notes that though "[t]he specific type of bus is not disclosed by Fujimoto . . . , there are two types of busses that

exist[s](sic) for this purpose, parallel or serial" (Ans. 17). The Examiner then concludes that "when the combination of Fujimoto and Millard is made there would be additional processors for the shared memory devices" and notes that such combination "would result in an interconnection of multiple processors, which Millard disclosed can be done with a serial bus" (Ans. 18).

Though in the Reply Brief, Appellant admits that "'Host IF' 102 [of Fujimoto] corresponds to the 'director device' of the claim," that "microprocessor 101 [of Fujimoto] would have to correspond to the 'command control unit' of the claim," and that "'shared memory device having a cache memory' . . . . would have to be the 'Cache Memory Unit' 14 described as having a cache memory 109 and controller 108" (Reply Br. 2), Appellant argues that "[t]here clearly is no serial bus interconnecting microprocessor 101 with CM controller 108" in Fujimoto (Reply Br. 3). Appellant contends that "the conventional wisdom for interconnecting two processors used for disk array devices is by way of using a shared bus" (Reply Br. 3). Thus, Appellant contends that "even if Millard were properly combinable with Fujimoto, there would still be no suggestion of providing a dedicated … high speed serial bus specifically for [the] purpose of transmitting commands and returned processing results" (Reply Br. 4 (emphasis omitted)).

Appellant's arguments that "Fujimoto does not have its two interfaces … controlled by a single entity" (App. Br. 13) and that there are "no suggestion of providing a dedicated … high speed serial bus specifically for [the] purpose of transmitting commands and returned processing results" (Reply Br. 4 (emphasis omitted)) are not commensurate in scope with the

recited language of claim 1. That is, claim 1 does not require a "single" entity controlling two interfaces or any bus "specifically for purpose of transmitting commands and returned processing results" as Appellant contends. Rather, claim 1 merely requires that the command control unit of the director device is connected to the command control unit of the shared memory device by a "serial communication bus." Further, since claim 1 does not define as to what a "director device" is to mean, include or represent, contrary to Appellant's argument (App. Br. 13), claim 1 does not preclude a "director device" that comprises a plurality of separate interfaces that perform separate functions. Accordingly, in this Appeal, we address whether the teachings of Fujimoto in view of Millard would have suggested a serial communication bus connecting a command control unit of a director device and a command control unit of a shared memory device, as specially required by claim 1.

Fujimoto discloses a disk array device comprising interfaces that manage input/output of data to/from an external device and a disk drive device (FF 1) and shared memory units including a cache memory for input/output data (FF 3), wherein the interfaces comprise microprocessors for controlling the data transaction with the shared memory units and the cache memory comprises a cache memory controller and a memory module (FF 2-3). We find Fujimoto's interfaces to comprise "a director device which manages input/output data to/from an external device and a disk drive device" and find Fujimoto's microprocessor of the interfaces as "a command control unit which transmits said command and receives a processing result" as recited in claim 1. We also find Fujimoto's shared memory units to comprise "a shared memory device having a cache memory for input/output

data" wherein the cache memory controller comprises "a processing unit which executes control of said cache memory" and "a command control unit which receives a command from said director device" as recited in claim 1. In fact, even Appellant admits that "'Host IF' 102 [of Fujimoto] corresponds to the 'director device' of the claim," that "microprocessor 101 [of Fujimoto] would have to correspond to the 'command control unit' of the claim," and that "'shared memory device having a cache memory' . . . . would have to be the 'Cache Memory Unit' 14 described as having a cache memory 109 and controller 108" (Reply Br. 2).

Furthermore, Fujimoto discloses that microprocessor 101 and host IF 102 are connected, whereby CM access controller 105 is connected to host IF 102 (FF 4). We find microprocessor 101 to be connected to CM access controller 105. Furthermore, CM access controller 105 is also connected to CM controller 108 (*id*). Accordingly, we find microprocessor 101 to be connected to CM controller 108 via CM access controller 105. Thus, we find Fujimoto discloses that the command control unit of a director device is connected to the command control unit of the shared memory device as required by claim 1.

We thus agree with the Examiner's finding that "Fujimoto describes the connections between all the components of the system" (Ans. 17). Further, we find no error with the Examiner's finding that, though "[t]he specific type of bus is not disclosed by Fujimoto . . . , there are two types of busses that exists for this purpose, parallel or serial" (Ans. 17). In fact, as Millard discloses, communications between processors, a host computer, an intelligent terminal or other processor devices may be on a serial or parallel basis (FF 6). That is, Millard discloses the use of direct communication bus

(serial or parallel) to enable high speed data transfer among the several processors included within the storage facility and also external host computers or intelligent terminals (FF 5-6).

Accordingly, we find no error in the Examiner's conclusion that Fujimoto in view of Millard would have suggested a serial communication bus connecting a command control unit of a director device and a command control unit of a shared memory device as required by claim 1. That is, contrary to Appellant's contention (App. Br. 12), we conclude that Fujimoto in view of Millard do at least suggest two command control units, wherein "a high speed serial bus interconnecting these two components" (App Br. 12) is provided therebetween.

Although Appellant also argues that, because "architectures are distinctly different from each other and from the claimed invention," the prior art teachings "preclude a conclusion of obviousness" (App. Br. 13), Appellant appears to have viewed the references from a different perspective than the Examiner. The issue here is not whether the ordinarily skilled artisan would have added Millard's system with Fujimoto's system but whether the artisan, upon reading Millard, would find it obvious to use a serial bus for high speed data transfer as the communication bus of Fujimoto. The Supreme Court has determined that the conclusion of obviousness can be based on the interrelated teachings of multiple patents, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

Here, both Fujimoto and Millard are directed to the same field of endeavor of cache memory control. We conclude that such application of Millard's serial bus for high speed data transfer as the bus for data transfer in Fujimoto is no more than a simple arrangement of old elements with each performing the same function it had been known to perform, yielding no more than one would expect from such an arrangement. *KSR*, 550 U.S. at 416. The skilled artisan would "be able to fit the teachings of multiple patents together like pieces of a puzzle" since the skilled artisan is "a person of ordinary creativity, not an automaton." *Id.* at 420-21. As stated by the Supreme Court, an obviousness "analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 418. *See also Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006).

Accordingly, we find that the Examiner did not err in rejecting independent claim 1 over Fujimoto in view of Millard.

As for independent claims 17, 26, and 29, Appellant merely repeats the claim language (App. Br. 16) but does not provide arguments separate from those of claim 1 (App. Br. 17-18). As discussed above with respect to claim 1 which recites similar features, we conclude that Fujimoto in view of Millard would have suggested the recited features. As a result, we find that the Examiner also did not err in rejecting independent claims 17, 26 and 29 over Fujimoto in view of Millard. Appellant does not provide arguments for claims 3-13, 16, 19-22, and 25, 27, 28, 30 and 31 separate from those of claims 1, 17, 26, and 29 from which they respectively depend, other than to

say "there are no corresponding configurations in the cited references, as required by claims 7-13" (App. Br. 18). Accordingly, claims 3-13, 16, 19-22, and 25, 27, 28, 30 and 31 fall with claims 1, 17, 26, and 29.

Claims 14, 15, 23, and 24

As for claims 14, 15, 23, and 24, Appellant merely contend that "these claims are allowable for at least the same reasons that their underlying base claims are allowable as set forth above" (App. Br. 18). As discussed above with respect to claims 1 and 17 from which claims 14, 15, 23 and 24 respectively depend, we find no error in the Examiner's rejection of the claims over Fujimoto in view of Millard. Accordingly, we find that the Examiner also did not err in rejecting independent claims 14, 15, 23 and 24 over Fujimoto and Millard in further view of Scaringella.

V. CONCLUSION AND DECISION

The Examiner's rejection of claims 1, 3-17, and 19-31 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

peb

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/372,198	03/10/2006	Atsushi Kuwata	MA-674-US	4344

21254 7590 02/23/2010

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EXAMINER	
DUDEK JR, EDWARD J	

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Appeal No: 2010-003807
Application: 11/372,198
Appellant: Atsushi Kuwata

Board of Patent Appeals and Interferences
Docketing Notice

Application 11/372,198 was received from the Technology Center at the Board on January 19, 2010 and has been assigned Appeal No: 2010-003807.

A review of the file indicates that the following documents have been filed by appellant:

Appeal Brief filed on:	July 13, 2009
Reply Brief filed on:	November 30, 2009
Request for Hearing filed on:	NONE

In all future communications regarding this appeal, please include both the application number and the appeal number.

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
11372198	3/10/2006	KUWATA, ATSUSHI	MA-674-US

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EXAMINER
Edward J. Dudek

ART UNIT	PAPER
2186	20100104

DATE MAILED:

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Commissioner for Patents

The reply brief filed 30 November 2009 has been entered and considered. The application has been forwarded to the Board of Patent Appeals and Interferences for decision on the appeal.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

/Edward J Dudek/
Examiner, Art Unit 2186

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Atsushi KUWATA

Serial No.:	11/372,198	Group Art Unit:	2186
Filed:	March 10, 2006	Examiner:	Dudek

For: DISK ARRAY DEVICE AND SHARED MEMORY DEVICE THEREOF, AND CONTROL PROGRAM AND CONTROL METHOD OF DISK ARRAY DEVICE

Commissioner of Patents
Alexandria, VA 22313-1450

APPELLANT'S REPLY BRIEF ON APPEAL

Sir:

Based on the new arguments and comments made of record by the Examiner for the first time during prosecution, Appellant respectfully submits the following reply to the Examiner's Answer mailed on September 30, 2009.

I. The rejection of record fails to establish a *prima facie* obviousness rejection by failing to demonstrate all elements of the claimed invention, based on primary reference Fujimoto

The claimed invention describes both structure and function in all of the independent claims. Therefore, the prior art evaluation must start out by assuming both the structure and function of the cited primary reference.

Appellant has repeatedly requested during prosecution that the Examiner take into account the structure of primary reference Fujimoto and then identify the

differences and provide a reasonable rationale to modify the structure that is demonstrated in Fujimoto to arrive at the structure of the claimed invention.

The evaluation of record does not follow this fundamental obviousness evaluation and, therefore, fails to provide a *prima facie* obviousness rejection.

Instead, the evaluation of record accounts only for functional similarities but ignores the structure of primary reference Fujimoto.

II. The following technical analysis based on primary reference Fujimoto clearly demonstrates that the Examiner has erred in the prior art evaluation

II(a). The structure clearly described by independent claim 1 requires a director device that manages the I/O of data from an external device and the disk drive device, where the director device has a command control unit that transmits the command for controlling of a cache memory and that receives a processing result.

The only structure in primary reference Fujimoto that would seem to reasonably satisfy this structural/functional description is shown in Figure 7 and would have to be the "Host IF" 102 that corresponds to the "director device" of the claim, and that includes microprocessor 101 that would have to correspond to the "command control unit" of the claim (e.g., see lines 6-9 of column 7).

II(b). Claim 1 also clearly describes a "shared memory device having a cache memory" and having a "processing unit" that executes control of the cache memory and that has a "command control unit" that receives commands from the director device's command control unit, and that transmits the processing result back to the command control unit.

The only structure in primary reference Fujimoto that would seem to reasonably satisfy this structural/functional description is shown in Figure 7 and would have to be the "Cache Memory Unit" 14 described as having a cache memory 109 and controller 108 (e.g., see lines 43-45 of column 7).

II(c). The final claim limitation of claim 1 also clearly describes that a serial bus interconnects the command control unit of the director device with the command control unit of the shared memory device.

There clearly is no serial bus interconnecting microprocessor 101 with CM controller 108 in Figure 7 of Fujimoto. Therefore, the Examiner has the initial burden of providing a reasonable rationale (e.g., one of the seven rationales set out in KSR) to modify the structure shown in Figure 7 of Fujimoto to incorporate a serial data bus between microprocessor 101 and CM controller 108.

The closest attempt in the rejection of record that attempts to address this aspect of the claimed invention the Examiner's new argument, presented for the first time in the Examiner's Answer in paragraph (10) on page 17:

"*The specific type of bus is not disclosed by Fujimoto, however, there are two types of busses that [exist] for this purpose, parallel or serial. Each bus has its own advantages, and it would have been obvious to try each of these busses, since there are a limited number of choices, in an attempt to solve the problem of connecting these devices together. Furthermore, when the combination of Fujimoto and Millard is made there would be additional processors for the shared memory devices. This would result in an interconnection of multiple processors, which Millard disclosed can be done with a serial bus (see column 2, line 60).*"

Appellant submits that there are at least three problems with the Examiner's new argument recited above and that this rationale is insufficient to demonstrate obviousness.

First, as explained in paragraph [0009] of the disclosure of the present application, the conventional wisdom for interconnecting two processors used for disk array devices is by way of using a shared bus. In contrast, the final limitation of the claimed invention explicitly requires that a serial communication bus be used for transmission of commands and processing results. All of the references of record, including primary reference Fujimoto, appear to follow this conventional architecture of using a shared bus.

Thus, contrary to the conventional wisdom in the art at the time of the invention, the claimed invention modifies the conventional architecture by separating

the bus functions between processors by providing a high speed serial bus dedicated to commands/processing results.

Neither Fujimoto nor Millard suggests separating bus functions in the manner described by the claimed invention. That is, neither reference suggests using a serial command bus in combination with the conventional shared bus that would remain to provide parallel data transmission between processors in a disk array device.

Therefore, even if Millard were considered to be properly combinable with Fujimoto, there would still be no suggestion of providing a dedicated a high speed serial bus specifically for purpose of transmitting commands and returned processing results. The claimed invention separates the transmission paths of data and commands, and uses a high speed serial bus specifically for the command bus, which is not taught or suggested in either cited reference.

Thus, the combination of the claimed invention is more than merely trying a serial bus as a shared bus versus using a parallel bus as the shared bus, as the Examiner alleges in his new argument. Indeed, using a serial bus to replace a parallel bus that is a shared bus would only slow down the overall shared bus transmission, absent some type of objective evidence by the Examiner, which evidence is not currently of record.

Second, as Appellant has repeatedly pointed out during prosecution, the details of the architecture of secondary reference demonstrate a completely different principle of operation from that of primary reference Fujimoto. It is, therefore, not properly combinable under the holding of *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), as described in MPEP 2143.01: "*If the proposed modification or combination would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious.*"

That is, the extraction of specific design features from two circuits operating under two fundamentally different principles of operation is clear indication of impermissible hindsight, unless the Examiner demonstrates that the extracted feature is reasonably either a direct substitution performing the identical function in both circuits or provides an improvement in the context of the circuit of the primary reference. In the final sentence on page 4 of the Examiner's Answer, the Examiner himself

characterizes secondary reference Millard as demonstrating a fundamentally different approach (*e.g.*, different principle of operation) from that of primary reference Fujimoto.

Stated slightly differently in the concepts of *KSR*, since circuits do not function as abstract ideas that can be freely rearranged based upon a roadmap of a claimed invention, extracting a design detail from two references having drastically different architectural details, even if both circuits arguably perform similar functions, would clearly violate the requirement of *KSR* that the Examiner demonstrate an expectation of success, since the primary reference already performs the similar function without any improvement or substitution of an element of a system having a drastically different configuration. Therefore, the modification of primary reference Fujimoto by Millard is improper in the rejection of record, since there is no reasonable motivation to modify the primary reference and no expectation of success absent impermissible hindsight.

Third, the description involving line 60 of column 2 of Millard, upon which the Examiner relies in the rejection of record, actually recites:

"*The communications level processor is configured to communicate with a host computer, an intelligent terminal or other processor devices on either a serial, parallel or DMA basis and performs all communications functions with such external devices, such as handshake, protocol and the like.*"

Appellant submits that the above-recited description makes no suggestion to incorporate a serial communication bus explicitly for purpose of transmitting commands and receiving processing results, and the most that can reasonably be concluded from the Examiner's new argument is that the Examiner concludes that the claimed invention would have been possible at the time of the invention.

The Examiner's allegation that "... *it would have obvious to try each of these busses, since there are a limited number of choices, in an attempt to solve the problem of connecting these devices together*" is not supported by objective evidence and does not arrive at the claimed invention, since it is specifically the command bus between two specific processors that is described as using the serial communication bus.

That is, the claimed invention involves more than "merely trying different buses", since it also includes separating the commands/responses from a shared bus

between two specific processors in a disk array device, and incorporating, instead, a serial bus dedicated to commands/responses, as well as using the conventional parallel data bus for the data between these two processors.

Stated slightly differently, if the Examiner's allegation were correct that it would be "obvious to try each of different busses", then there would clearly be no burden on the Examiner to demonstrate, by objective evidence, at least one example of such configuration described in the independent claims. The failure to provide any objective evidence is clear indication of improper hindsight.

Thus, the Examiner's newly-articulated reliance on "obvious to try" is clearly misplaced, since the Appellant's own evaluation above demonstrates that the element missing from primary reference Fujimoto is more than a mere substitution of allegedlly "obvious to try" alternatives.

That is, rather than merely "trying" a serial bus rather than a parallel bus, a key difference between the claimed invention and primary reference Fujimoto is that the shared bus of the conventional architectural wisdom is modified to provide a high speed serial bus dedicated to transporting command/process reports between two of the processors in a disk array device. None of the references of record demonstrate this claim element, and the rejection of record fails to properly identify this difference.

III. The evaluation of record fails to comply with the requirements set forth in *KSR* describing that the Examiner has the initial burden to identify the differences from the primary reference (*i.e.*, Fujimoto) and then provide an articulation of a reasonable rationale to modify that primary reference to arrive at the claimed invention

That is, in ignoring the structure described in the claimed invention, the rejection of record has also failed to properly recognize the differences between primary reference Fujimoto and the claimed invention, since the claimed invention involves more than the mere replacement of the shared bus demonstrated in the prior art references. Rather, the claimed invention actually describes two processors in a disk array device having a bus dedicated to commands and process reports.

The Examiner's new argument based on "obvious to try" is misplaced, since the difference between Fujimoto and the independent claims is not a simple substitution of

a limited number of known alternatives. Rather, the claimed invention involves a modification to the shared bus conventionally used in disk array devices.

CONCLUSION

In view of the foregoing, Appellant submits that the Examiner has clearly erred in the rejections currently of record and that claims 1, 3-17, and 19-31, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. Thus, the Board is respectfully requested to reverse all rejections of claims 1, 3-17, and 19-31.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Attorney's Deposit Account number 50-0481.

Respectfully submitted,

Dated: 11/30/09

Frederick E. Cooperrider
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TRANSMITTAL FORM

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Application Number	11/372,198
Filing Date	March 10, 2006
First Named Inventor	Atsushi KUWATA
Art Unit	2186
Examiner Name	Edward J. Dudek, Jr.
Attorney Docket Number	MA-674-US

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
- ☐ Fee Attached
- ☐ Amendment / Reply
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
- ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
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- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to TC
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- ☒ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	McGinn Intellectual Property Law Group, PLLC 8321 Old Courthouse Road, Suite 200, Vienna, Virginia 22182		
Signature			
Printed name	Frederick E. Cooperrider, Esq.		
Date	November 30, 2009	Reg. No.	36,769

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/372,198	03/10/2006	Atsushi Kuwata	MA-674-US	4344

21254 7590 10/20/2009

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EXAMINER	
DUDEK JR, EDWARD J	
ART UNIT	**PAPER NUMBER**
2186	

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
11372198	3/10/2006	KUWATA, ATSUSHI	MA-674-US

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EXAMINER
Edward J. Dudek

ART UNIT	PAPER
2186	20091019

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Commissioner for Patents

The information disclosure statement (IDS) submitted on 20 April 2009 and 16 September 2009 were filed after the mailing date of the advisory action on 05 March 2009. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

/Edward J Dudek/
Examiner, Art Unit 2186

/Pierre-Michel Bataille/
Primary Examiner, Art Unit 2186

Receipt date: 04/20/2009

APR 20 2009 PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number	GAU: 2186
MA-674-US	11/372,198	

Applicant(s): Atsushi KUWATA

Filing Date	Group Art Unit
March 10, 2006	2186

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,477,619 B1 already of record	11/05/2002	Fujimoto et al.			
		6,915,389 B2	07/05/2005	Fujimoto			

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
		2000-10900 A	01/14/2000	Japan			ABS	
		2001-256003 A	09/21/2001	Japan			ABS	
		2003-280824 A	10/02/2003	Japan			ABS	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Japanese Office Action February 2, 2009 with Partial English-Language Translation

EXAMINER	DATE CONSIDERED
/Edward Dudek Jr/	09/28/2009

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /EJD/

Receipt date: 09/16/2009

INFORMATION DISCLOSURE CITATION

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APPLICANT(S)	11372198 - GAU: 2186
Atsushi KUWATA	
FILING DATE	GROUP ART UNIT
March 10, 2006	2186

U.S. PATENT DOCUMENTS

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U.S. PATENT APPLICATION PUBLICATIONS

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		2002-328850	11/15/2002	Japan			Abs	
		2002-351622	12/06/2002	Japan			Abs	
		2004-171177	06/17/2004	Japan			Abs	
		2004-213125	07/29/2004	Japan			Abs	
		2004-240949	08/26/2004	Japan			Abs	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			Japanese Office Action dated June 16, 2009 (with partial English translation).

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MA-674-US	11/372,198
Atsushi KUWATA	11372198 - GAU: 2186
FILING: **March 10, 2006**	GROUP ART: **2186**

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		2005-011277	01/13/2005	Japan			Abs	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED
/Edward Dudek Jr/	09/28/2009

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11/372,198	03/10/2006	Atsushi Kuwata	MA-674-US	4344

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11372198	3/10/2006	KUWATA, ATSUSHI	MA-674-US

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EXAMINER
Edward J. Dudek

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Commissioner for Patents

The information disclosure statements (IDS) submitted on 20 April 2009 and 16 September 2009 were filed after the mailing date of the advisory action on 05 March 2009. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

/Matt Kim/
SPE, AU2186

/Edward J Dudek/
Examiner, Art Unit 2186

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11/372,198	03/10/2006	Atsushi Kuwata	MA-674-US	4344

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 11/372,198
Filing Date: March 10, 2006
Appellant(s): KUWATA, ATSUSHI

Frederick E. Cooperrider
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 13 July 2009 appealing from the Office action mailed 03 December 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 23 February 2009 has been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,477,619	Fujimoto	11-2002
6,467,047	Scaringella	10-2002
4,096,567	Millard	06-1978

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

An after final amendment was filed on 19 February 2009, and was entered, as it simply moved a limitation from a dependent claim into the independent claim. The grounds of rejection have been modified to address this limitation, regarding the serial bus that was presented in dependent claim 3, in the independent claims that now contain this limitation.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-13, 16-17, 19-22, and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (**U.S. Patent #6,477,619**) in view of Millard (**U.S. Patent #4,096,567**).

As per claim 1: Fujimoto discloses a disk array device comprising a director device which manages input/output of data to/from an external device and a disk drive device **(see column6, lines 42-56)**, and a shared memory device having a cache memory for input/output data **(see column 6, lines 42-56)**, wherein said director device transmits a command for instructing on control of the cache memory for said input/output data to said shared memory device, and said shared memory device executes control of said cache memory for said input/output data based on a command from said director device **(see column 9, lines 45-54 and column 10, lines 1-6)**, wherein said director device includes a command control unit which transmits said command and receives a processing result for said command **(see column 9, lines 18-26 and 45-54 and column 10, lines 1-6)**, and a command control unit which receives a command from said director device and transmits a processing result for said command **(see column 10, lines 1-6)**. Fujimoto fails to disclose the result is sent from the shared memory device and the shared memory device includes a processing unit which executes control of said cache memory for said input/output data based on a command from said director device, and wherein the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus. Milliard discloses a multilayer processor system whereby processing and data access functions are divided up into multiple level, and each level

has a processor and command queue to perform a specific function thereby relieving a higher level processor from the task and allowing the higher level processor to continue work on another task **(see abstract)**. When a requesting processor has to perform a search of a cache memory or other storage for data that is needed by a program, the processor must suspend execution of the program, search for the data, load all parts of the data, then resume execution **(see column 2, lines 1-35)**. This causes significant delay in the execution of the program **(see column 2, lines 1-35)**. Therefore Millard discloses multiple processing levels to allow the host processor to continue working while the lower processing levels carry out the data searching **(see column 2, lines 38-45)**. The multiple processors at the multiple levels can be connected by a serial communication bus **(see column 2, line 60)**. The system is designed around an mailbox system so that a higher level processor will send a request to the lower level processors mailbox, the lower level processor will then perform the actions required, then send a response back to the requestors mailbox **(see column 3, lines 10-50)**. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Fujimoto to include a processor in the shared memory unit so the channel IF unit is not required to search the cache for the requested data, thereby allowing the channel IF to process more commands, and to have the shared memory unit send responses back and fourth when its job it done, as disclosed by Millard, this will then relieve the channel IF processors and the Disk IF processors from having to stop their work, search the cache memory, and then resume their work and create a more efficient system, as taught by Millard.

As per claim 3: the command control units of said director device and said shared memory device transmit and receive information related to a state of said cache memory **(see column 9, lines 35-55)**.

As per claim 4: wherein said director device includes a communication buffer unit **(see Millard column 3, lines 10-25)**, and said director device is released from control operation for said shared memory device upon storage of said command in said communication buffer **(see column 2, lines 38-46)**.

As per claim 5: wherein said director device receives a processing result for said command **(see Fujimoto column 10, lines 1-6)** which is sent from said shared memory device at said communication buffer **(see Millard column 3, lines 35-50)**.

As per claim 6: wherein said shared memory device includes a communication buffer unit which receives and stores said command sent from said director device and stores a processing result for said command **(see Millard column 3, lines 10-25)**.

As per claim 7: comprising: said director device and said shared memory device in plural **(see Fujimoto column 8, lines 35-40)**, wherein the plurality of said director devices and the plurality of said shared memory devices are connected with each other through said command control units **(see Fujimoto column 8, lines 35-40)**.

As per claim 8: wherein said director device includes a communication buffer, said communication buffer receiving a plurality of processing results for said commands which are sent from the plurality of said memory devices **(see Millard column 3, lines 35-50)**.

As per claim 9: wherein the plurality of said shared memory devices each include a communication buffer unit which receives said commands sent from the plurality of said director devices and stores a processing result for said commands **(see Fujimoto column 7, lines 45-55 and Millard column 3, lines 35-50)**.

As per claim 10: wherein the plurality of said director devices are separately formed as a host director device which accepts a data request from said external device and other director device to which said disk drive device is connected **(see Fujimoto column 6, lines 42-56)**.

As per claim 11: wherein the plurality of said director devices are each formed to be connected to said external device and said disk drive device **(see column 6, lines 42-56)**.

As per claim 12: said director device in plural and single said shared memory device **(Fujimoto already discloses a single shared memory see figure 7, elements 13 and 14, an one director device, see figure 7, there is no patentable significance of duplicating the director device unless there are unexpected results gained from such a configuration see MPEP 2144.04 (VI)(A) and In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960))**, wherein the plurality of said director devices transmit, to a processing unit of said shared memory device, a command instructing on control of the cache memory **(see Fujimoto column 9, lines 25-35)**.

As per claim 13: single said director device and said shared memory devices in plural **(Fujimoto already discloses a single shared memory see figure 7, elements 13 and 14, an one director device, see figure 7, there is no patentable significance**

of duplicating the shared memory device unless there are unexpected results gained from such a configuration see MPEP 2144.04 (VI)(A) and In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960)), wherein said director device transmits, to the plurality of said shared memory devices, a command instructing on control of the cache memory **(see Fujimoto column 9, lines 25-35)**.

As per claim 16: wherein said director device and said shared memory device are separately formed to be individual devices **(see Fujimoto column 6, lines 42-56)**.

As per claim 17: Fujimoto discloses A shared memory device of a disk array device including a director device which manages input/output of data to/from an external device and a disk drive device **(see column6, lines 42-56)**; a shared memory device having a cache memory for input/output data **(see column 7, lines 35-45)**; a command control unit which receives said command transmitted from a command control unit of said director device and transmits a processing result for said command to the command control unit of said director device **(see column 9, lines 45-54 and column 10, lines 1-6)**, wherein based on a command for instructing on control of the cache memory for said input/output data which is transmitted from said director device, control of said cache memory for said input/output data is executed **(see column 9, lines 45-54 and column 10, lines 1-6)**. Fujimoto fails to disclose the result is sent from the shared memory device and the shared memory device includes a processing unit which executes control of said cache memory for said input/output data based on a command from said director device, and the command control unit of the shared

memory device being connected to the command control unit of said director device by a serial communication bus. Milliard discloses a multilayer processor system whereby processing and data access functions are divided up into multiple level, and each level has a processor and command queue to perform a specific function thereby relieving a higher level processor from the task and allowing the higher level processor to continue work on another task **(see abstract)**. When a requesting processor has to perform a search of a cache memory or other storage for data that is needed by a program, the processor must suspend execution of the program, search for the data, load all parts of the data, then resume execution **(see column 2, lines 1-35)**. This causes significant delay in the execution of the program **(see column 2, lines 1-35)**. Therefore Millard discloses multiple processing levels to allow the host processor to continue working while the lower processing levels carry out the data searching **(see column 2, lines 38-45)**. The multiple processors at the multiple levels can be connected by a serial communication bus **(see column 2, line 60)**. The system is designed around a mailbox system so that a higher level processor will send a request to the lower level processors mailbox, the lower level processor will then perform the actions required, then send a response back to the requestors mailbox **(see column 3, lines 10-50)**. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Fujimoto to include a processor in the shared memory unit so the channel IF unit is not required to search the cache for the requested data, thereby allowing the channel IF to process more commands, and to have the shared memory unit send responses back and fourth when its job it done, as

disclosed by Millard, this will then relieve the channel IF processors and the Disk IF processors from having to stop their work, search the cache memory, and then resume their work and create a more efficient system, as taught by Millard.

As per claim 19: transmits and receives information related to a state of said cache memory to/from the command control unit of said director device **(see column 9, lines 35-55)**.

As per claim 20: comprising: a communication buffer unit which receives and stores said command sent from said director device and stores a processing result for said command **(see Millard column 3, lines 35-50)**.

As per claim 21: comprising: said director device and said shared memory device in plural **(see Fujimoto column 8, lines 35-40)**, wherein the plurality of said director devices and the plurality of said shared memory devices are connected with each other through said command control units **(see Fujimoto column 8, lines 35-40)**.

As per claim 22: wherein the plurality of said shared memory devices each include a communication buffer unit which receives said commands sent from the plurality of said director devices and stores a processing result for said commands **(see Fujimoto column 7, lines 45-55 and Millard column 3, lines 35-50)**.

As per claim 25: which is formed as an individual device separately from said director device **(see Fujimoto column 6, lines 42-56)**.

As per claim 26: Fujimoto discloses a programmable medium tangibly embodying control program for controlling input/output of data in a disk array device including a

director device which manages input/output of data to/from an external device and a disk drive device **(see column6, lines 42-56)**, and a shared memory device having a cache memory for said input/output data **(see column 7, lines 35-45)**, said control program being executed on a processor of said director device and having the functions of: transmitting, from the processor of said director device, a command for instructing said shared memory device to control the cache memory for said input/output data, and causing said shared memory device to execute control of said cache memory for said input/output data based on a command from said director device **(see column 9, lines 45-54 and column 10, lines 1-6)**. Fujimoto fails to disclose a processor as part of the shared memory device and that the processor of the shared memory device executes control of the shared memory device, and that the commands are transmitted between the processor and director device via a high speed serial bus. Milliard discloses a multilayer processor system whereby processing and data access functions are divided up into multiple level, and each level has a processor and command queue to perform a specific function thereby relieving a higher level processor from the task and allowing the higher level processor to continue work on another task **(see abstract)**. When a requesting processor has to perform a search of a cache memory or other storage for data that is needed by a program, the processor must suspend execution of the program, search for the data, load all parts of the data, then resume execution **(see column 2, lines 1-35)**. This causes significant delay in the execution of the program **(see column 2, lines 1-35)**. Therefore Millard discloses multiple processing levels to allow the host processor to continue working while the lower processing levels carry out

the data searching **(see column 2, lines 38-45)**. The multiple processors at the multiple levels can be connected by a serial communication bus **(see column 2, line 60)**. The system is designed around a mailbox system so that a higher level processor will send a request to the lower level processors mailbox, the lower level processor will then perform the actions required, then send a response back to the requestors mailbox **(see column 3, lines 10-50)**. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Fujimoto to include a processor in the shared memory unit so the channel IF unit is not required to search the cache for the requested data, thereby allowing the channel IF to process more commands, and to have the shared memory unit send responses back and fourth when its job it done, as disclosed by Millard, this will then relieve the channel IF processors and the Disk IF processors from having to stop their work, search the cache memory, and then resume their work and create a more efficient system, as taught by Millard.

As per claim 27: which realizes: in the processor of said director device, the function of transmitting said command and receiving a processing result for said command which is sent from said shared memory device **(see Fujimoto column 10, lines 1-6)**, and in the processor of said shared memory device, the function of executing control of said cache memory for said input/output data based on a command from said director device **(see Fujimoto column 9, lines 18-26)**, and the function of receiving a command from said director device and transmitting a processing result for said command from said shared memory device **(see Millard column 3, lines 35-50)**.

As per claim 28: which realizes for the processor of said director device and the processor of said shared memory device, the function of transmitting and receiving information related to a state of said cache memory between said director device and said shared memory device **(see Fujimoto column 9, lines 25-35)**.

As per claim 29: Fujimoto discloses a control method of controlling input/output of data in a disk array device including a director device which manages input/output of data to/from an external device and a disk drive device **(see column6, lines 42-56)**, and a shared memory device having a cache memory for said input/output data **(see column 7, lines 35-45)**, comprising: the step of transmitting, from a processor of said director device, a command for instructing said shared memory device to control the cache memory for said input/output data, and the step of said shared memory device to execute control of said cache memory for said input/output data based on a command from said director device **(see column 9, lines 45-54 and column 10, lines 1-6)**. Fujimoto fails to disclose a processor as part of the shared memory device and that the processor of the shared memory device executes control of the shared memory device, and the commands are transmitted and received between the processor and the director device via a high speed serial bus. Milliard discloses a multilayer processor system whereby processing and data access functions are divided up into multiple level, and each level has a processor and command queue to perform a specific function thereby relieving a higher level processor from the task and allowing the higher level processor to continue work on another task **(see abstract)**. When a requesting

processor has to perform a search of a cache memory or other storage for data that is needed by a program, the processor must suspend execution of the program, search for the data, load all parts of the data, then resume execution **(see column 2, lines 1-35)**. This causes significant delay in the execution of the program **(see column 2, lines 1-35)**. Therefore Millard discloses multiple processing levels to allow the host processor to continue working while the lower processing levels carry out the data searching **(see column 2, lines 38-45)**. The multiple processors at the multiple levels can be connected by a serial communication bus **(see column 2, line 60)**. The system is designed around a mailbox system so that a higher level processor will send a request to the lower level processors mailbox, the lower level processor will then perform the actions required, then send a response back to the requestors mailbox **(see column 3, lines 10-50)**. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by Fujimoto to include a processor in the shared memory unit so the channel IF unit is not required to search the cache for the requested data, thereby allowing the channel IF to process more commands, and to have the shared memory unit send responses back and fourth when its job it done, as disclosed by Millard, this will then relieve the channel IF processors and the Disk IF processors from having to stop their work, search the cache memory, and then resume their work and create a more efficient system, as taught by Millard.

As per claim 30: wherein the processor of said director device includes the step of transmitting said command and receiving a processing result for said command

which is sent from said shared memory device **(see Fujimoto column 10, lines 1-6)**, and the processor of said shared memory device includes the steps of executing control of said cache memory for said input/output data based on a command from said director device **(see Fujimoto column 9, lines 18-26)**, and receiving a command from said director device and transmitting a processing result for said command from said shared memory device **(see Millard column 3, lines 35-50)**.

As per claim 31: transmitting and receiving information related to a state of said cache memory between said director device and said the processor of said shared memory device **(see Fujimoto column 9, lines 25-35)**.

Claims 14-15 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Fujimoto (**U.S. Patent #6,477,619**) and Millard (**U.S. Patent #4,096,567**) as applied to claims 1, 3-13, 16-17, 19-22, and 25-31 above, and further in view of Scaringella (**U.S. Patent #6,467,047**).

As per claim 14: the combination of Fujimoto and Millard disclose all the limitations of claim 1 as discussed above. The combination fails to disclose said shared memory device is provided with a parity operation unit which executes parity operation processing for data of said cache memory in processing of write back to said disk drive device. Scaringella discloses a storage system and high reliability and high performance controllers for a storage system. Since storage systems often store critical data, reliability is very important in the operation of the system **(see column 1, lines 45-60)**. The system contains a cache memory and also a parity memory for generating

and checking the parity of the data being read from the storage system and data being written to the storage system **(see column 2, lines 5-65)**. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by the combination of Fujimoto and Millard to have the shared memory device include a parity memory for generating and checking the parity of the data in the storage system so the system would be highly reliable and perform well, as taught by Scaringella.

As per claim 15: said parity operation unit is connected to said cache memory by other path than a data transfer path of said cache memory **(see figure 3, element 212)**.

As per claim 23: the combination of Fujimoto and Millard disclose all the limitations of claim 17 as discussed above. The combination fails to disclose said shared memory device is provided with a parity operation unit which executes parity operation processing for data of said cache memory in processing of write back to said disk drive device. Scaringella discloses a storage system and high reliability and high performance controllers for a storage system. Since storage systems often store critical data, reliability is very important in the operation of the system **(see column 1, lines 45-60)**. The system contains a cache memory and also a parity memory for generating and checking the parity of the data being read from the storage system and data being written to the storage system **(see column 2, lines 5-65)**. It would have been obvious to a person having ordinary skill in the art to which said subject matter pertains to have modified the system disclosed by the combination of Fujimoto and Millard to have the

shared memory device include a parity memory for generating and checking the parity of the data in the storage system so the system would be highly reliable and perform well, as taught by Scaringella.

As per claim 24: said parity operation unit is connected to said cache memory by other path than a data transfer path of said cache memory **(see figure 3, element 212)**.

(10) Response to Argument

Response to arguments regarding claims 1, 3-13, 16-17, 19-22, and 25-31

Appellant argues "For example, there is no demonstration of: '… wherein the command control unit of said director device is connected to the command control unit of said shared memory device by a serial communication bus', as required by independent claims 1 and 17, with the process claims incorporating similar language. Likewise, the Examiner points to no specific structure in the cited references, let alone structure that is interconnected in the manner described by the claims while still performing the functions described." (See page 11)

The Examiner respectfully disagrees. Fujimoto describes the connections between all the components of the system (see column 7, lines 5-35). Specifically lines 15-20 and lines 30-35 disclose these elements as being interconnected by a communication bus. The specific type of bus is not disclosed by Fujimoto, however, there are two types of busses that exists for this purpose, parallel or serial. Each bus has its own advantages, and it would have been obvious to try each of these busses, since there are a limited number of choices, in an attempt to solve the problem of

connecting these devices together. Furthermore, when the combination of Fujimoto and Millard is made there would be additional processors for the shared memory devices. This would result in an interconnection of multiple processors, which Millard disclosed can be done with a serial bus (see column 2, line 60).

Appellant argues "More specifically, the claimed invention has an architecture 100 in which the interface functions 111, 112 between the host computer 101 and the disk drive devices 102, 103, 104, are segregated from the cache function included in the shared memory device 12. The two interfaces 111, 112 (i.e., one interface 111 for the host computer 101 and one interface 112 for the disk drive devices 102, 103, and 104) are controlled by a first processor 113, and the cache function is controlled by a second processor unit 122. This combination of elements is not present in either Fujimoto or Millard. Therefore, even if primary reference Fujimoto and secondary reference Millard are also directed to disk drive storage having at least one cache, their architectures are distinctly different from each other and from the claimed invention. Primary reference Fujimoto does not have its two interfaces (e.g., the channel IF unit 11 and the disk IF unit 12) controlled by a single entity such as the director device of the claimed invention, as required by the plain meaning of the language of independent claim 1." (See page 13)

The Examiner respectfully disagrees. Fujimoto consists of disk array controllers that are all interconnected to each other and function to control accesses to disk drives from host computers (see figure 5, elements 1-2). Each disk array controller contains

multiple distinct elements that work together to accomplish this functionality (see figure 7). There is a channel IF unit that provides connectivity to the host computers and a disk IF unit that provides connectivity to the disk drives (see figure 7, elements 11 and 12. These units have a dedicated interface for the hosts and the disks, elements 102 and 103. They also contain microprocessors to perform the work, element 101. See also column 7, lines 5-35). These two units work independently of each other. There is also a shared memory unit and a cache memory unit that receives command from each of these interface units (see figure 7, elements 13, 14, 107, and 108), and returns the requested data to the interface units (see column 9, lines 23-25 and lines 30-35). All these components are under control of the disk array control unit. Fujimoto discloses the same configuration of physical components that are set forth in the independent claims. Fujimoto fails to disclose having some of these components controlled by one entity, and other components controlled by a different entity. In Fujimoto, the shared memory devices and the cache memory devices have their own controllers, but the access commands are sent from the processors in the host interface and disk interface units (see column 9, lines 18-26). Therefore, the processors in the host and disk interfaces in Fujimoto are essentially controlling accesses to the memories and the subsequent actions when data is not located in the memories. Millard is used to disclose the limitations regarding having some of these components controlled by one entity, and other components controlled by a different entity.

Appellant argues “According to the Examiner's opinion, the three-processor-level configuration of secondary reference Millard constitutes an improvement over the configuration of Fujimoto. Regardless of whether one agrees with the Examiner's opinion, it is clear that modification of Fujimoto to incorporate the three-processor-level configuration of Millard, considered by the Examiner to be an improvement, involves a drastic change in configuration to Fujimoto, since it requires, as a minimum, adding a second cache level and drastically reconfiguring the interconnections of the components of Millard. Such change in principle of operation is improper under the holding of In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), as described in MPEP §2143.01: ‘If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious.” (See page 14)

The system of Milliard discloses the use of multiple processors working together to accomplish a task rather than having a single processor perform all the work alone. Typically the storage units connected to the host computer had no processing capability, and the host computer was responsible for controlling and accessing the storage devices. When the host was busy accessing the storage, the processor could not service other requests, since the processor was tied up accessing the storage. Millard adds another processing level to the storage system to allow the host computer to send requests to the storage system. The processor at the storage system can now perform the functions required to satisfy the request while the host computer processor can service other requests while waiting for the response (see column 2, lines 38-45).

In Fujimoto, this same situation occurs, there is a processor in the channel IF unit and the disk IF unit, and they send commands to the shared memory and cache memory to look for data. If the data is not there, then the same processor must now send another command to another disk array controller to find the data. Sending these multiple requests ties up the processor from servicing other requests that are received at the interfaces. The teaching of Millard can remedy this situation in the same way. Adding a processor to control the shared memory units and the cache memory units of Fujimoto would allow the processors in the channel IF unit and disk IF unit to send a single request to the memory units, and the processors in the memory units can then do the necessary work and send any additional commands that are needed to retrieve the requested data. In the meantime, the processors for the channel IF and disk IF can be processing other requests that are received at the IF units. This modification does not change the principle of operation of Fujimoto. The operations of the disk array controllers would remain the same, the only change would be a redistribution of the workload across more processors.

Appellant argues “First of all, each of independent claims 1, 17, 26, and 29 recite that the processor of the shared memory unit controls the cache memory. However, in Fujimoto, shared memory units 13 are separate from cache memory units 14, and thus are presumably controlled through interface units 11. Thus, there is no apparent control connection between shared memory units 13 and cache memory units 14 such that shared memory units 13 can control cache memory units 14 as recited in the claimed

invention. Along those lines, even if shared memory units 13 of Fujimoto included the processor of Millard as suggested in the Office Action, there would still be no way for shared memory units 13, with or without the processor, to exert control over cache memory units 14 as recited in the claimed invention." (See page 17)

The Examiner respectfully disagrees. In the system of Fujimoto, when data is requested, the processor of the channel IF unit sends a command to the shared memory unit to determine if the data requested is in the cache memory. If the data is there, another command is issued to transfer the data from the cache and to the host computer. If the data is not in the cache, the microprocessor issues another command to another processor to read the data out of the disk array and store the data in the cache. There is also a link between the shared memory and the cache memory since the shared memory unit contains information as to what data is currently in the cache memory (see figure 7, element 111 and column 8, lines 18-32). The shared memory unit is the device that is searched to determine if the requested data is in the cache memory. Millard discloses multiple processing levels to allow the host processor, in this case the processor of the channel IF unit, to continue working while the lower processing levels carry out the data searching. By using this methodology, and incorporating a processor into the shared memory unit, some of the workload can be relieved from the channel IF processor. The processor of the shared memory unit would be capable of receiving a command from the channel processor indicating that data is requested. The shared memory unit would then be able to search the cache and return the data if the data is present, or forward a command to another channel

processor to get the data from the disk drive, and then forward the data when it is received. This way, the channel processor would no longer have to deal with finding the data, as the processor of the shared memory unit would take care of that, and the channel processor could continue satisfying other requests that it receives. Since there is already a link between the shared memory unit and the cache memory, a processor in the shared memory unit would be more than capable of controlling the cache to perform I/O.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Examiner, Art Unit 2186

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