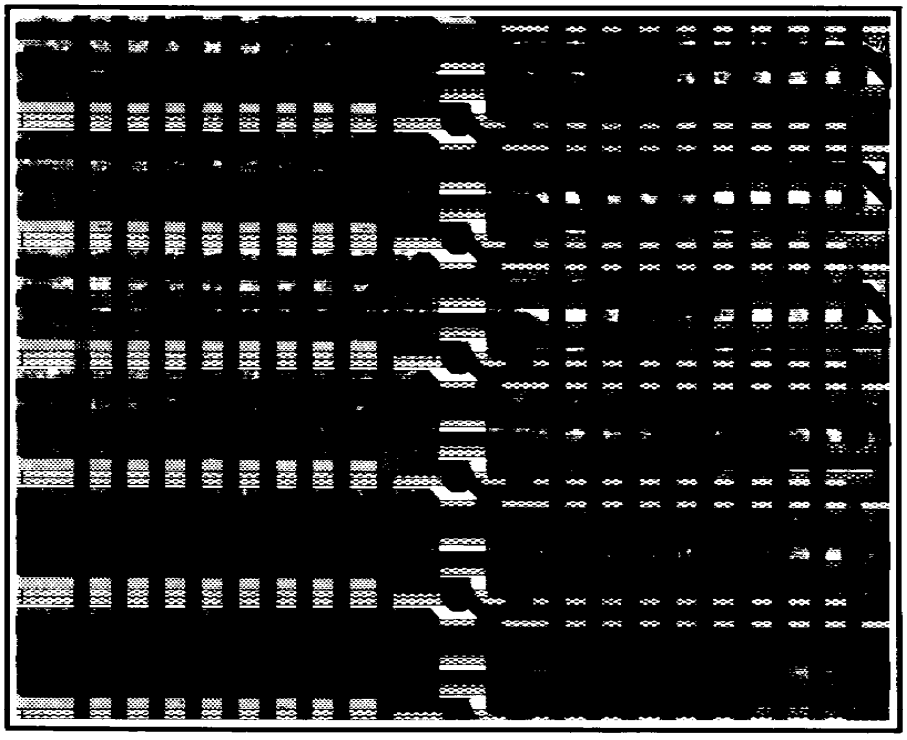
Appendix C

SEMICONDUCTOR MEMORIES

A Handbook of Design, Manufacture, and Application

Second Edition



Betty Prince

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Semiconductor Memories

A Handbook of Design, Manufacture and Application

Second Edition

Betty Prince
Texas Instruments, USA

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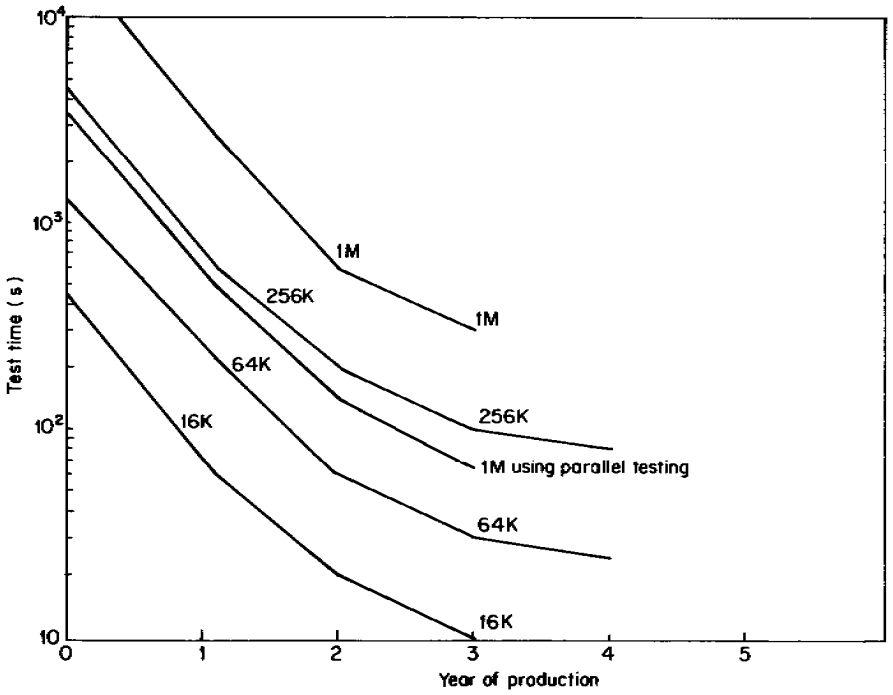


Figure 14.1
Final test time for various DRAM densities by year of production (assuming similar test flow).

Highly sophisticated test algorithms have been developed with the aim of reducing test time while maintaining the required quality.

Figure 14.1 illustrates test timing improvements for various densities of DRAMs from the point of device introduction followed by an engineering experience curve until an optimum and stable situation is reached in about the third year of production.

The average test time required for the different types of MOS memory products varies considerably. DRAMs and SRAMs of similar densities have similar test times. Products such as EPROMs take a factor of 10 increase in test time. Since test time impacts the throughput of the product line and is allocated in overhead on expensive test equipment it adds considerably to the cost of production. Figures 14.2(a) and (b) show memory test equipment being used.

14.2 FAILURE MODES AND TEST PATTERNS

The rapid growth in circuit complexity has greatly increased the difficulty and cost of testing memories.

Semiconductor memory testing can be basically reduced to four different groups:

Cell test Every cell must be capable of storing a logic '0' and a logic '1' for a given minimum amount of time and, if the memory is writable, must be capable of being changed from one state to the other.

(a)

(b)

Figure 14.2
Examples of memory test. (a) Volume production final electrical test showing memory test machines and handlers. (b) Sample electrical test at outgoing inspection. ([60] 1990, with permission of NMB Semiconductor.)

Data in–out test Sense lines and data in–out lines must be capable of recovering from read–write operations. Sense amplifiers have to operate within the small, specified voltage or charge levels.

Address decoder test Every cell must be correctly and uniquely addressed by the decode logic.

Disturb testing The accessing of one part of the memory array must not affect any other part.

Special test Functions specified for different memory types must be checked and verified operational. This will include the testing of control lines such as chip enable, output enable, chip select, or special logic circuits.

The design of a sequence of test patterns to check the necessary failure condition for a memory device calls for not only thorough component knowledge, but also an in-depth understanding of various MOS failure mechanisms.

It is important to test for the maximum number of failure modes for the test pattern chosen, while at the same time avoiding combinations of standard patterns which result in double testing, or in checking for unnecessary conditions.

A few common memory failure modes highlighting the above failure groups are listed.

- Cell: 'stuck-at' failures, open or short circuits, leakage, adjacent cell disturbance.
- Access times: minimum and maximum to specification.
- Address decoder: open or short circuits, noise, high sensitivity.
- Sense amplifier: recovery time.
- Refresh times: minimum.
- Clocks.
- Write: recovery time.

'Stuck-at' cell failures are one of the commonest forms of failure. In this mode the single cell bit is simply 'stuck' at '1' or '0'. Complex tests are not necessary to determine this type of failure.

Additional failure modes specifically related to different memory families also have to be screened for and will add to the above list.

A variety of standard test patterns are commonly used for screening out most known failures. Figure 14.3(a) illustrates some test pattern types with corresponding test time constants and failure descriptions.

The test time required is calculated by substituting N with memory size (or number of bits) followed by multiplication by the cycle time used. It can be seen that most tests fall within three different categories: $2N$, $2N^{3/2}$, or N^2. Test time is mostly dependent on memory size, cycle time, and test pattern performed.

Figure 14.3(b) illustrates test times as a function of memory size for $2N$, $2N^{3/2}$, and $2N^2$ type patterns.

A typical test pattern sequence might include the following.

1. All '1' or all '0'.
2. Checkerboard

Pattern	Constant	Failure
March	$10N$	Cell access
Walking pattern	$2(N^2 + N)$	Multiple address sense amplifier recovery
Galloping pattern	$2(N^2 + N)$	Multiple address sense amplifier recovery
Sliding diagonal	$2(3N^{3/2} + 5N)$	Cell testing, diagonal
Galloping column	$2(3N^{3/2} + 6N)$	Cell testing, columns

(a)

Pattern	1k	4k	16k	64k	256k
$2N$	0.41	1.64	6.55	26.2	76.8
$2N^{3/2}$	13.57	104.8	839	6710.9	53,687
$2N^2$	439	6710.9	107 347	1717 987	27 487 792

(b)

Figure 14.3
(a) Typical test patterns with corresponding test time constants and failure descriptions 'N' is the device bit density. (b) Illustrative test times as a function of density. (Reproduced with permission of John Wiley.)

3. Stripe
4. Marching
5. Galloping
6. Sliding diagonal
7. Waling
8. Ping-Pong.

Numbers 1 to 4 are called 'N' patterns. These can check one sequence of N bits of memory by at most using the given pattern several times. Numbers 5 to 7 are called N^2 patterns. These need several times of N^2 patterns to check one sequence of N bits of memory. N^2 patterns have a long test time for high density memories. For example, a 64k RAM takes about 30 minutes to test with a galloping pattern and a 1Mb RAM takes over 6 hours.

The first three patterns in the sequence shown can check the array but are not sufficient to check the decoder circuits. The marching pattern is the simplest pattern which will check out the function of the memory. A description follows as an example of a typical marching diagonal test pattern.

A marching pattern is a pattern in which '1's march into all '0's. The procedure is as follows.

1. Clear all bits to '0'.
2. Read '0' from '0'th address and check that read data are '0'.
3. Write '1' on 0th address.
4. Read '0' from 1st address, and check read data are '0'.

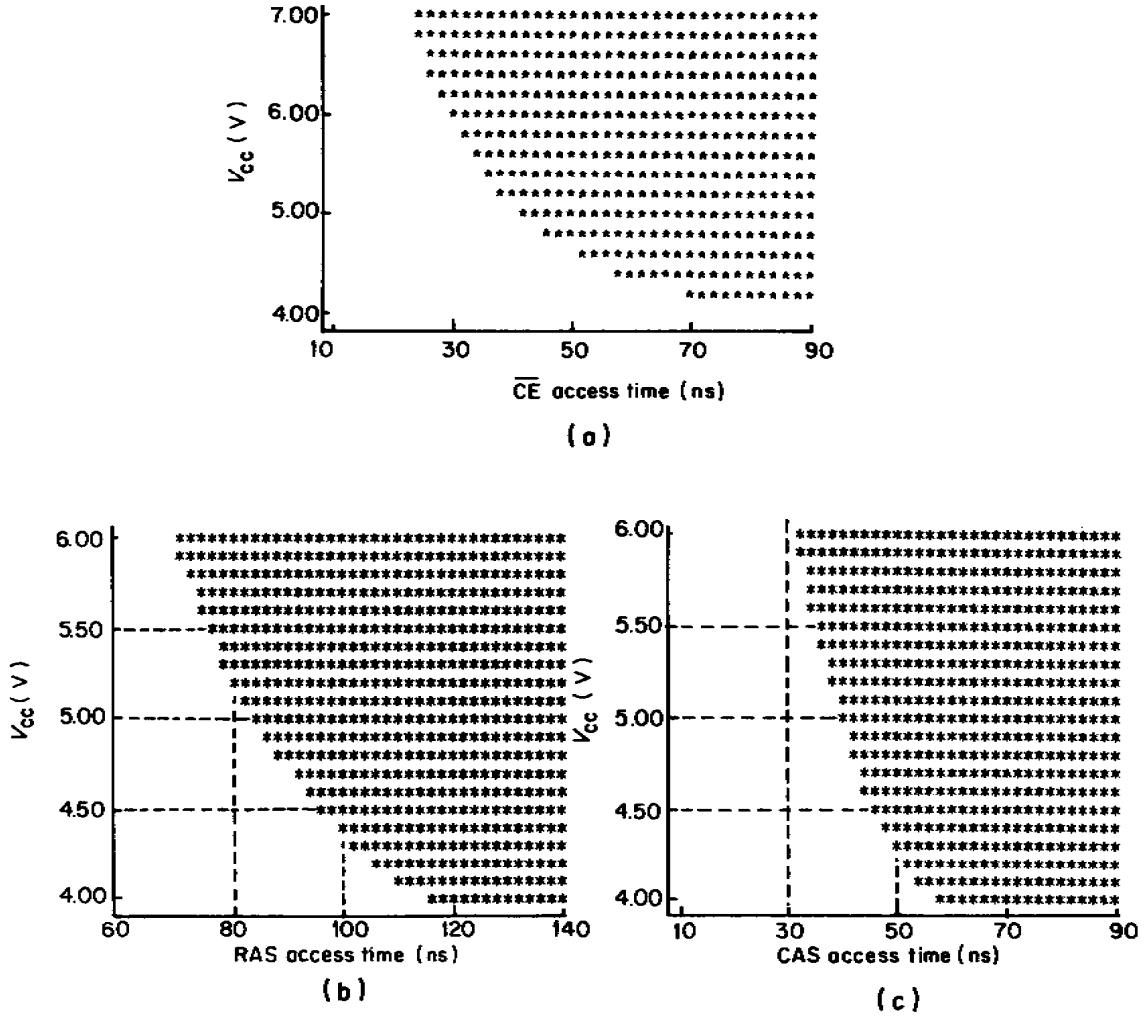


Figure 14.4
Various Shmoo plots showing functional device parameter regions for DRAMs. (a) V_{CC} plotted against $\overline{CE}$ (From Benevit *et al.* [37], AT & T 1982, with permission of IEEE), (b) V_{CC} plotted against $\overline{RAS}$, (c) V_{CC} plotted against $\overline{CAS}$. (From Kantz [45], Siemens 1984, with permission of IEEE.)

5. Write '1' on 1st address.
6. Repeat for N addresses until all are '1's.
7. Repeat 2 to 6 reading '1's and writing '0's until all data are '0'.

The commonest kind of 'stuck-at' failures can be found by this type of test. Test information can be presented as follows.

- Shmoo plots show the interaction between device parameters by plotting the range of functional parameter sets. Figure 14.4(a) shows the relation between V_{CC} and $\overline{CE}$ access time on a 256k DRAM. The plot shows a 40 ns chip enable access time at 5 V for the device under test. Figure 14.4(b) shows V_{CC} as a function of $\overline{RAS}$ access time and Figure 14.4(c) shows V_{CC} as a function of $\overline{CAS}$ access time.

  Asterisks denote the regions where the part is functional. Shmoos are generally used for device characterization, intersystem correlation, test program development, process and device correlation, and failure analysis.

- Accumulative Shmoo plots are derived from superimposing several Shmoos from different components.

- Wafer mapping is shown in Figure 14.5(a). This is used for probe yield analysis, wafer fabrication defects analysis, mask defect analysis, alignment problems, and system correlation. This is an accumulative representation of several wafers where the total failures for each die location are given as a percentage.

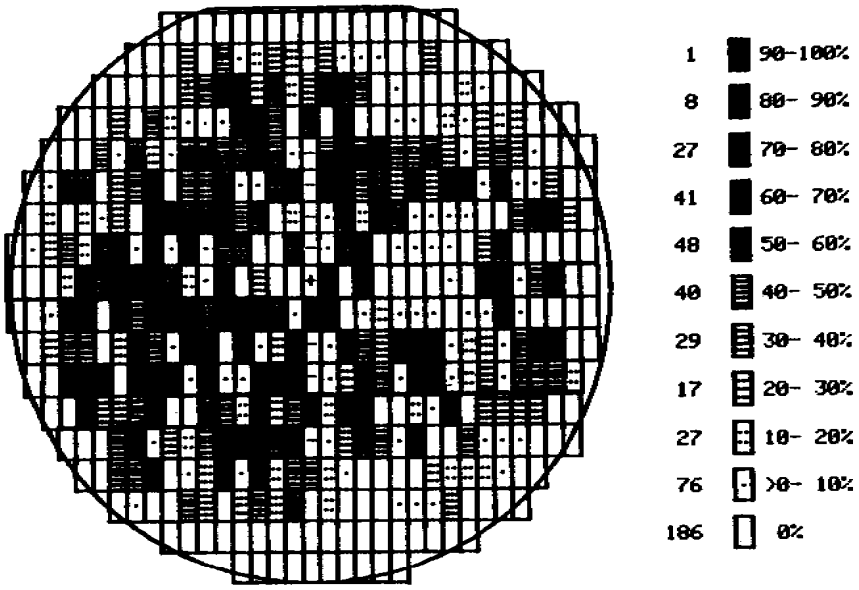
- Bit mapping: this gives fail–pass information for every bit or cell location of the memory under test. The results can be displayed on a color graphics terminal or printed. Real time bit mapping is fast and very effective during failure analysis, process evaluation, probe yield enhancement, pattern sensitivity detection, data retention (EPROMs) testing, pattern verification (ROMs) and device characterization. Figure 14.5(b) for example, shows a bit map of a 16k RAM as a 178 by 178 matrix. The vertical dotted line illustrates a number of faulty bits.

14.3 TESTING DRAMs AND SRAMs

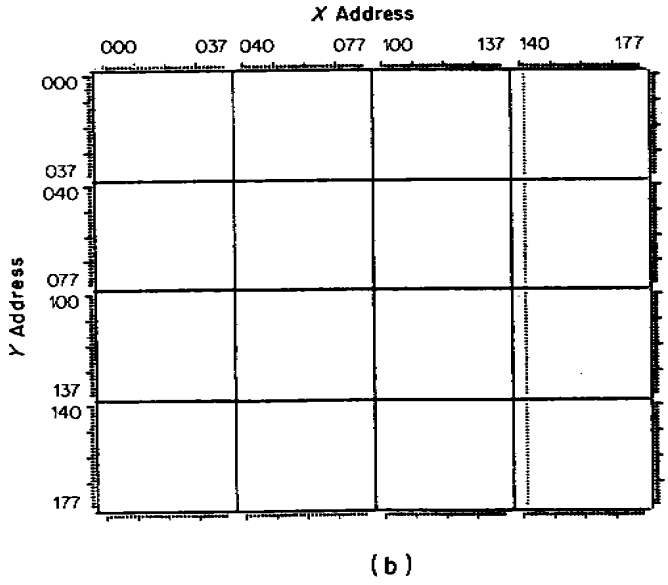
The various memory types of families such as ROMs, EPROMs, or RAMs will have different testing requirements due to differences in device characteristics, failure mechanisms, and operating modes. We will discuss special test considerations for dynamic and static RAMs, EPROMs, EEPROMs, and embedded memories.

14.3.1 Fault coverage considerations

The major problem in RAM testing is obtaining good fault coverage. As RAM density increases and advanced technologies and circuit techniques bring with them more complex failure modes, testing time increases rapidly.



(a)



(b)

Figure 14.5
(a) Wafer mapping of 16k DRAM. (b) Bit map of 16k DRAM. (From Prince and Due-Gundersen [64] 1983.)

For example a simple sliding diagonal test requires several hours to perform on a single 1Mb RAM chip. The more complex galloping pattern (GALPAT) test requires a testing time proportional to N^2 for an N-bit RAM. If testing a 1k RAM takes a few seconds, then testing a 1Mb RAM may require several days. The extent of fault coverage in these tests is also not easy to define.

Table 14.1 Normalized test times for dynamic RAMs.

Density	Normalized test time
65k	1.0
256k	3.1
1M	10.4

Normalized test times for various generations of DRAM are shown in Table 14.1 taken from a paper by TI [50] where the test time of the 64k DRAM is taken as '1' and it is assumed that the same test flow is used for all. If 8 bit parallel testing is used for the 1Mb DRAM then the test time is reduced from a factor of 10.4 to 2.0. Parallel testing is described more fully in the later section on DRAM test modes.

14.3.2 Failure modes

Most failure modes related to RAMs are well known with corresponding test patterns for effective testing. Typical RAM failure modes include

- 'stuck at' faults
- pattern sensitivity
- multiple writing
- refresh sensitivity (DRAMs)
- open–short circuits
- leakage current faults
- sense amplifier recovery
- access time
- voltage bump (DRAMs)

A combination of well known $N^{3/2}$ and N type test patterns will generally provide the solution to effective screening for most of these failure modes. When the characteristics of a specific device are known it is often possible to delete parts of the initial test program and obtain a substantial reduction of test times.

Mechanisms, which are frequently involved in these failure modes, are reviewed below.

Gate oxide defects can cause stuck-at faults such as stuck-at 0, stuck-at word line, bit-word line crosstalk, transmission line effects, and row decoder failures.

The major sources of pattern sensitive failure modes in DRAMs are neighborhood interference faults, sense amplifier recovery problems and bit-line imbalance faults.

Neighborhood interference faults are frequently due to leakage current mechanisms

which can depend on the pattern of stored data in the neighboring cells. When the leakage current flowing between one cell and another is sufficient to destroy the contents of the cell, a neighborhood interference fault is said to occur. The worst case is when all surrounding cells have the opposite state to the tested cell.

Sense amplifier recovery problems can be caused by parasitic capacitance and resistance, which can also cause slow sense amplifiers, and transmission line effects. Sense amplifier recovery faults occur when, after repeated writing of the same cell, the data read out from that cell are independent of the contents of the cell.

Bit-line imbalance faults are caused by the difference in the total leakage associated with the cells connected to the two bit-lines involved.

14.3.3 Voltage bump test for DRAMs

Voltage bumping, or fluctuations of the power supply voltage, can cause erroneous data to be read out of the RAM. The voltage bump problem demands some special testing and the voltage bump test is a particularly rigorous test for a DRAM.

A positive V-bump is defined as V_{CC} during the write operation being lower than V_{CC} during the read operation. This fluctuation of V_{CC} lowers the read out voltage from the memory cell and may cause a read error.

If a V_{CC} level cell plate is used, the positive V-bump raises the stored level in the cell. Since the dummy cell level is kept at V_{SS} in spite of the bump, a low level in the cell may read erroneously as a high level.

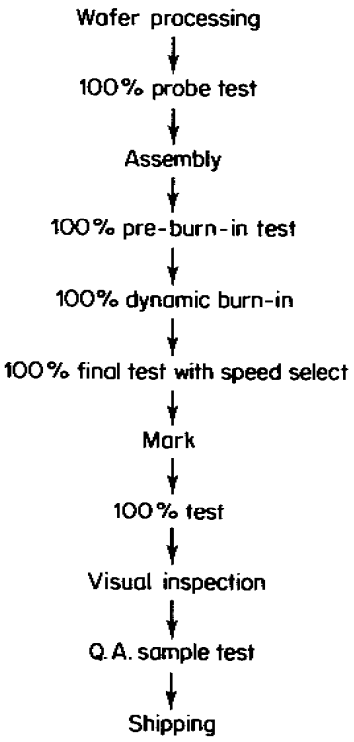


Figure 14.6
Typical dynamic RAM production flow charts. (From Prince and Due-Gundersen [64] 1983.)